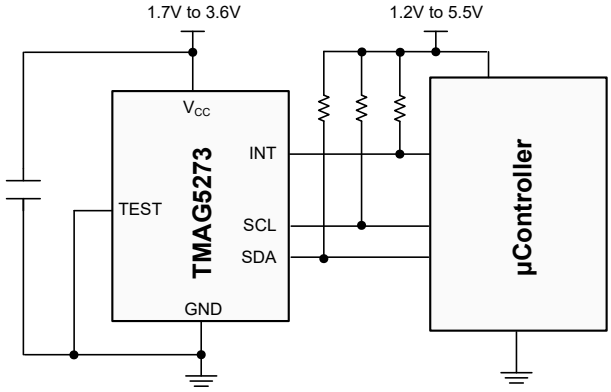
TMAG5273 3-Axis Linear Hall Effect Sensor With I²C Interface

1 Features

- 5% (Typical) Sensitivity Drift Across Operating Temperature
- Integrated Temperature Compensation for Multiple Magnet Types
- Selectable Linear Magnetic Sensitivity Range at X, Y, or Z Axis:
  - TMAG5273A1: ±40 mT, ±80 mT
  - TMAG5273A2: ±133 mT, ±266 mT
- Maximum 1-MHz I²C Clock Speed
- Cyclic Redundancy Check (CRC) with I²C Read
- Maximum 20-Ksps Sensing Bandwidth per Axis
- Interrupt Pin for Conversion Trigger and Status Update
- Integrated Angle CORDIC calculation with Gain and Offset Adjustment
- 1.7-V to 3.6-V Supply Voltage V_{CC} Range

2 Applications

- Electricity Meters
- Electronic Smart Lock
- Smart Thermostat
- Joystick & Gaming Controllers
- Drone Payload Control
- Door & Window Sensor
- Magnetic Proximity Sensor
- Mobile Robot Motor Control
- E-Bike



Application Block Diagram

3 Description

The TMAG5273 is a 3-Axis (3D) linear Hall effect sensor designed for wide range of industrial and personal electronics applications. This device integrates 3 independent Hall sensors in X, Y, and Z axes. A precision analog signal-chain along with integrated 12-bit AD converter digitizes the measured analog magnetic field values. The I²C interface, while supporting multiple operating V_{CC} ranges, ensures seamless data communications with low-voltage microcontrollers. The device integrated temperature sensor data is available for multiple system functions, such as thermal budget check or temperature compensation calculation for a given magnetic field.

The TMAG5273 can be configured to enable any magnetic fields and temperature measurements at any order required for a particular application. The device supports user defined interrupt and conversion trigger functions either through a dedicated $\overline{\text{INT}}$ pin, or through I2C line. Threshold detection features, along with wake up from sleep mode, enable flexible system design to optimize speed versus power consumption. Multiple diagnostics features enhance system design robustness and data integrity.

The device is offered in two different orderables for separate magnetic field ranges. Each orderable part can be configured further to select one of two magnetic field ranges that suits the magnet strength and component placements during system calibration. The high level of integration provides flexibility and cost effectiveness in a wide array of sensing system implementations.

The device performs consistently across a wide ambient temperature range of –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMAG5273	DBV (6)	2.9 mm × 1.6 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

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4 Revision History

DATE	REVISION	NOTES
June 2021	*	Initial release.

5 Pin Configuration and Functions

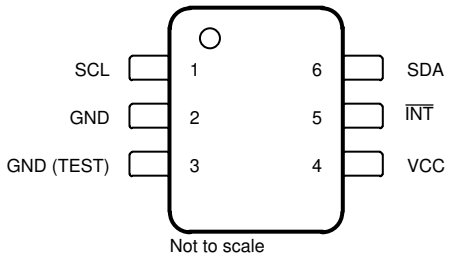

Figure 5-1. DBV Package 6-Pin SOT-23) Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
SCL	1	IO	Serial clock.
GND	2	Ground	Ground reference.
GND (TEST)	3	Input	TI Test Pin. Connect to ground in application.
VCC	4	Power supply	Power supply.
$\overline{\text{INT}}$	5	IO	Interrupt input/ output. If not used and connected to ground, set MASK_INTB = 1b.
SDA	6	IO	Serial data.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Main supply voltage	–0.3	4	V
I_{OUT}	Output current, SDA, $\overline{INT}$	0	10	mA
V_{OUT}	Output voltage, SDA, $\overline{INT}$	–0.3	7	V
V_{IN}	Input voltage, SCL, SDA, $\overline{INT}$	–0.3	7	V
B_{MAX}	Magnetic flux density		Unlimited	T
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	170	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)
over recommended V_{CC} range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Main supply voltage	1.7		3.6	V
V_{OUT}	Output voltage, SDA, $\overline{INT}$	0		5.5	V
I_{OUT}	Output current, SDA, $\overline{INT}$			2	mA
V_{IH}	Input HIGH voltage, SCL, SDA, $\overline{INT}$	0.7			V_{CC}
V_{IL}	Input LOW voltage, SCL, SDA, $\overline{INT}$			0.3	V_{CC}
T_A	Operating free air temperature	–40		125	C

6.4 Thermal Information

THERMAL METRIC(1)		TMAG5273 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	162	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	50.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	30.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	49.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)
over recommended V_{CC} range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA, $\overline{INT}$						
V_{OL}	Output LOW voltage, SDA, $\overline{INT}$ pin	I_{OUT} = 2mA	0		0.4	V
I_{OZ}	Output leakage current, SDA, $\overline{INT}$ pin	Output disabled, V_{OZ} = 5.5V	0		100	nA
$t_{FALL\_\overline{INT}}$	$\overline{INT}$ output fall time	R_{PU} =10KΩ, C_L =20pF, V_{PU} =1.65V to 5.5V		6		ns
$t_{INT\ (\overline{INT})}$	$\overline{INT}$ Interrupt time duration during pulse mode	INT_MODE =001b or 010b		10		µs
$t_{INT\ (SCL)}$	SCL Interrupt time duration	INT_MODE =011b or 100b		10		µs
DC POWER SECTION						
VCC_{UV} (1)	Under voltage threshold at V_{CC}	V_{CC} = 2.3V to 3.6V	1.9	2.0	2.2	V
I_{ACTIVE}	Active mode current	X, Y, Z, or thermal sensor active conversion, LP_LN =0b		2.3		mA
I_{ACTIVE}	Active mode current	X, Y, Z, or thermal sensor active conversion, LP_LN =1b		2.7		mA
$I_{STANDBY}$	Stand-by mode current	Device in trigger mode, no conversion started		0.45		mA
I_{SLEEP}	Sleep mode current			5		nA
AVERAGE POWER DURING DUTY-CYCLE MODE						
$I_{CC\_DCM\_1000\_1}$	Duty-cycle mode current consumption	Wake-up interval 1-ms, magnetic 1-ch conversion, LP_LN =0b, V_{CC} =3.3V		153		µA
$I_{CC\_DCM\_1000\_1}$	Duty-cycle mode current consumption	Wake-up interval 1-ms, magnetic 1-ch conversion, LP_LN =0b, V_{CC} =1.8V		152		µA
$I_{CC\_DCM\_1000\_4}$	Duty-cycle mode current consumption	Wake-up interval 1-ms, 4-ch conversion, LP_LN =0b, V_{CC} =3.3V		227		µA
$I_{CC\_DCM\_1000\_4}$	Duty-cycle mode current consumption	Wake-up interval 1-ms, 4-ch conversion, LP_LN =0b, V_{CC} =1.8V		227		µA
$I_{CC\_DCM\_0p2\_1}$	Duty-cycle mode current consumption	Wake-up interval 1000-ms, magnetic 1-ch conversion, LP_LN =0b, V_{CC} =3.3V		1.23		µA
$I_{CC\_DCM\_0p2\_1}$	Duty-cycle mode current consumption	Wake-up interval 1000-ms, magnetic 1-ch conversion, LP_LN =0b, V_{CC} =1.8V		0.88		µA
$I_{CC\_DCM\_0p2\_4}$	Duty-cycle mode current consumption	Wake-up interval 1000-ms, 4-ch conversion, LP_LN =0b, V_{CC} =3.3V		1.25		µA
$I_{CC\_DCM\_0p2\_4}$	Duty-cycle mode current consumption	Wake-up interval 1000-ms, 4-ch conversion, LP_LN =0b, V_{CC} =1.8V		0.9		µA

(1) The DIAG_STATUS and VCC_UV_ER bits are not valid for V_{CC} < 2.3V

6.6 Temperature Sensor

over operating free-air temperature range (unless otherwise noted)
over recommended V_{CC} range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SENS_RANGE}	Temperature sensing range		–40		170(1)	C
T_{ADC_T0}	Temperature result in decimal value (from 16-bit format) for T_{SENS_T0}			17508		
T_{SENS_T0}	Reference temperature for T_{ADC_T0}			25		C
T_{ADC_RES}	Temp sensing resolution (in 16-bit format)			60.1		LSB/C
NRMS_T	RMS (1 Sigma) temperature noise	CONV_AVG = 000b		0.4		C

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over operating free-air temperature range (unless otherwise noted)
over recommended V_{CC} range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NRMS_T	RMS (1 Sigma) temperature noise	CONV_AVG = 101b		0.2		C

(1) TI recommends not to exceed the specified operating free air temperature per the *Recommended Operating Conditions* table

6.7 Magnetic Characteristics For A1

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$B_{IN\_A1\_X\_Y}$	Linear magnetic range	X_Y_RANGE =0b		±40		mT
$B_{IN\_A1\_X\_Y}$	Linear magnetic range	X_Y_RANGE =1b		±80		mT
$B_{IN\_A1\_Z}$	Linear magnetic range	Z_RANGE =0b		±40		mT
$B_{IN\_A1\_Z}$	Linear magnetic range	Z_RANGE =1b		±80		mT
$SENS_{40\_A1}$	Sensitivity, X, Y, or Z axis	±40 mT range		820		LSB/mT
$SENS_{80\_A1}$	Sensitivity, X, Y, or Z axis	±80 mT range		410		LSB/mT
$SENS_{ER\_PC\_25C\_A1}$	Sensitivity error, X, Y, Z axis	TA =25C		±5.0%	±20.0%	
$SENS_{ER\_PC\_TEMP\_A1}$	Sensitivity drift from 25C, X, Y, Z axis			±5.0%		
$SENS_{LER\_XY\_A1}$	Sensitivity Linearity Error, X, Y-axis	TA =25C		±0.10%		
$SENS_{LER\_Z\_A1}$	Sensitivity Linearity Error, Z axis	TA =25C		±0.10%		
$SENS_{MS\_XY\_A1}$	Sensitivity mismatch among X-Y axes	TA =25C		±0.50%		
$SENS_{MS\_Z\_A1}$	Sensitivity mismatch among Y-Z, or X-Z axes	TA =25C		±1.0%		
$SENS_{MS\_DR\_XY\_A1}$	Sensitivity mismatch drift X-Y axes			±5%		
$SENS_{MS\_DR\_Z\_A1}$	Sensitivity mismatch drift Y-Z, or X-Z axes			±15%		
B_{off_A1}	Offset	TA =25C		±300	±1000	µT
$B_{off\_TC\_A1}$	Offset drift			±3.0	±10.0	µT/°C
$N_{RMS\_XY\_00\_000\_A1}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	LP_LN =0b, CONV_AVG = 000, TA =25C		±125		µT
$N_{RMS\_XY\_01\_000\_A1}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	LP_LN =1b, CONV_AVG = 000, TA =25C		±110		µT
$N_{RMS\_XY\_00\_101\_A1}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	LP_LN =0b, CONV_AVG = 101, TA =25C		±31		µT
$N_{RMS\_XY\_01\_101\_A1}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	LP_LN =1b, CONV_AVG = 101, TA =25C		±28		µT
$N_{RMS\_Z\_00\_000\_A1}$	RMS (1 Sigma) magnetic noise (Z axis)	LP_LN =0b, CONV_AVG = 000, TA =25C		±45		µT
$N_{RMS\_Z\_01\_000\_A1}$	RMS (1 Sigma) magnetic noise (Z axis)	LP_LN =1b, CONV_AVG = 000, TA =25C		±41		µT
$N_{RMS\_Z\_00\_101\_A1}$	RMS (1 Sigma) magnetic noise (Z axis)	LP_LN =0b, CONV_AVG = 101, TA =25C		±11		µT
$N_{RMS\_Z\_01\_101\_A1}$	RMS (1 Sigma) magnetic noise (Z axis)	LP_LN =1b, CONV_AVG = 101, TA =25C		±9		µT
$A_{ERR\_Y\_Z\_101\_A1\_25}$	Y-Z Angle error in full 360 degree rotation	CONV_AVG = 101, TA =25C		±1.0		Degree
$A_{ERR\_X\_Z\_101\_A1\_25}$	X-Z Angle error in full 360 degree rotation	CONV_AVG = 101, TA =25C		±1.0		Degree
$A_{ERR\_X\_Y\_101\_A1\_25}$	X-Y Angle error in full 360 degree rotation	CONV_AVG = 101, TA =25C		±0.5		Degree

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6.8 Magnetic Characteristics For A2

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$B_{IN\_A2\_X\_Y}$	Linear magnetic range	X_Y_RANGE =0b		±133		mT
$B_{IN\_A2\_X\_Y}$	Linear magnetic range	X_Y_RANGE =1b		±266		mT
$B_{IN\_A2\_Z}$	Linear magnetic range	Z_RANGE =0b		±133		mT
$B_{IN\_A2\_Z}$	Linear magnetic range	Z_RANGE =1b		±266		mT
$SENS_{133\_A2}$	Sensitivity, X, Y, or Z axis	±133 mT range		250		LSB/mT
$SENS_{266\_A2}$	Sensitivity, X, Y, or Z axis	±266 mT range		125		LSB/mT
$SENS_{ER\_PC\_25C\_A2}$	Sensitivity error, X, Y, Z axis	TA = 25C		±5.0%	±20.0%	
$SENS_{ER\_PC\_TEMP\_A2}$	Sensitivity drift from 25C, X, Y, Z axis			±5.0%		
$SENS_{LER\_XY\_A2}$	Sensitivity Linearity Error, X, Y-axis	TA =25C		±0.10%		
$SENS_{LER\_Z\_A2}$	Sensitivity Linearity Error, Z axis	TA =25C		±0.10%		
$SENS_{MS\_XY\_A2}$	Sensitivity mismatch among X-Y axes	TA =25C		±0.50%		
$SENS_{MS\_Z\_A2}$	Sensitivity mismatch among Y-Z, or X-Z axes	TA =25C		±1.0%		
$SENS_{MS\_DR\_XY\_A2}$	Sensitivity mismatch drift X-Y axes			±5%		
$SENS_{MS\_DR\_Z\_A2}$	Sensitivity mismatch drift Y-Z, or X-Z axes			±15%		
B_{off_A2}	Offset	TA =25C		±300	±1000	µT
$B_{off\_TC\_A2}$	Offset drift			±3.0	±10	µT/°C
$N_{RMS\_XY\_00\_000\_A2}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	LP_LN =0b, CONV_AVG = 000, TA =25C		±150		µT
$N_{RMS\_XY\_01\_000\_A2}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	LP_LN =1b, CONV_AVG = 000, TA =25C		±145		µT
$N_{RMS\_XY\_01\_101\_A2}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	LP_LN =0b, CONV_AVG = 101, TA =25C		±37		µT
$N_{RMS\_XY\_10\_101\_A2}$	RMS (1 Sigma) magnetic noise (X or Y-axis)	LP_LN =1b, CONV_AVG = 101, TA =25C		±34		µT
$N_{RMS\_Z\_00\_000\_A2}$	RMS (1 Sigma) magnetic noise (Z axis)	LP_LN =0b, CONV_AVG = 000, TA =25C		±75		µT
$N_{RMS\_Z\_10\_000\_A2}$	RMS (1 Sigma) magnetic noise (Z axis)	LP_LN =1b, CONV_AVG = 000, TA =25C		±71		µT
$N_{RMS\_Z\_00\_101\_A2}$	RMS (1 Sigma) magnetic noise (Z axis)	LP_LN =0b, CONV_AVG = 101, TA =25C		±19		µT
$N_{RMS\_Z\_10\_101\_A2}$	RMS (1 Sigma) magnetic noise (Z axis)	LP_LN =1b, CONV_AVG = 101, TA =25C		±16		µT
$A_{ERR\_Y\_Z\_101\_A2}$	Y-Z Angle error in full 360 degree rotation	CONV_AVG = 101, TA =25C		±1.0		Degree
$A_{ERR\_X\_Z\_101\_A2}$	X-Z Angle error in full 360 degree rotation	CONV_AVG = 101, TA =25C		±1.0		Degree
$A_{ERR\_X\_Y\_101\_A2}$	X-Y Angle error in full 360 degree rotation	CONV_AVG = 101, TA =25C		±0.50		Degree

6.9 Magnetic Temp Compensation Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TC_{00}	Temperature compensation (X, Y, Z-axes)	MAG_TEMPCO =00b		0		%/°C
TC_{12}	Temperature compensation (X, Y, Z-axes)	MAG_TEMPCO =01b		0.12		%/°C
TC_{20}	Temperature compensation (X, Y, Z-axes)	MAG_TEMPCO =11b		0.2		%/°C

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6.10 I²C Interface Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I²C Interface Fast Mode Plus (V_{CC} =2.3V to 3.6V)						
f_{I2C_fmp}	I²C clock (SCL) frequency	LOAD = 50 pF, V_{CC} =2.3V to 3.6V			1000	KHz
t_{whigh_fmp}	High time: SCL logic high time duration		350			ns
t_{wlo_wfmp}	Low time: SCL logic low time duration		500			ns
$t_{su\_cs\_fmp}$	SDA data setup time		50			ns
$t_{h\_cs\_fmp}$	SDA data hold time		120			ns
t_{icr_fmp}	SDA, SCL input rise time				120	ns
t_{icf_fmp}	SDA, SCL input fall time				55	ns
$t_{h\_ST\_fmp}$	Start condition hold time		0.1			µs
$t_{su\_SR\_fmp}$	Repeated start condition setup time		0.1			µs
$t_{su\_SP\_fmp}$	Stop condition setup time		0.1			µs
$t_{w\_SP\_SR\_fmp}$	Bus free time between stop and start condition		0.2			µs
I²C Interface Fast Mode (V_{CC} =1.7V to 3.6V)						
f_{I2C}	I²C clock (SCL) frequency	LOAD = 50 pF, V_{CC} =1.7V to 3.6V			400	KHz
t_{whigh}	High time: SCL logic high time duration		600			ns
t_{wlow}	Low time: SCL logic low time duration		1300			ns
t_{su_cs}	SDA data setup time		100			ns
t_{h_cs}	SDA data hold time		0			ns
t_{icr}	SDA, SCL input rise time				300	ns
t_{icf}	SDA, SCL input fall time				300	ns
t_{h_ST}	Start condition hold time		0.3			µs
t_{su_SR}	Repeated start condition setup time		0.3			µs
t_{su_SP}	Stop condition setup time		0.3			µs
$t_{w\_SP\_SR}$	Bus free time between stop and start condition		0.6			µs

6.11 Power up & Conversion Time

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{start\_power\_up}$	Time to go to stand-by mode after V_{CC} supply voltage crossing V_{CC_MIN}			270		µs
t_{start_sleep}	Time to go to stand-by mode from sleep mode(1)			50		µs
$t_{start\_measure}$	Time to go into continuous measure mode from stand-by mode			80		µs
$t_{measure}$	Conversion time(2)	CONV_AVG = 000b, OPERATING_MODE =10b, only one channel enabled		50		µs
$t_{measure}$	Conversion time(3)	CONV_AVG = 101b, OPERATING_MODE =10b, only one channel enabled		825		µs
t_{go_sleep}	Time to go into sleep mode after SCL goes high			20		µs

(1) The device will recognize the I²C communication from a primary only during stand-by or continuous measure modes. While the device is in sleep mode, a valid secondary address will wake up the device but no acknowledge will be sent to the primary. Start up time need to be considered before addressing the device after wake up.

(2) Add 25µs for each additional magnetic channel enabled for conversion with CONV_AVG = 000b. When CONV_AVG = 000b, the conversion time doesn't change with the T_CH_EN bit setting.

(3) For conversion with CONV_AVG =101b, each channel data is collected 32 times. If an additional channel is enabled with CONV_AVG =101b, add 32×25µs = 800µs to the $t_{measure}$ to calculate the conversion time for two channels.

6.12 Typical Characteristics

at T_A = 25°C typical (unless otherwise noted)

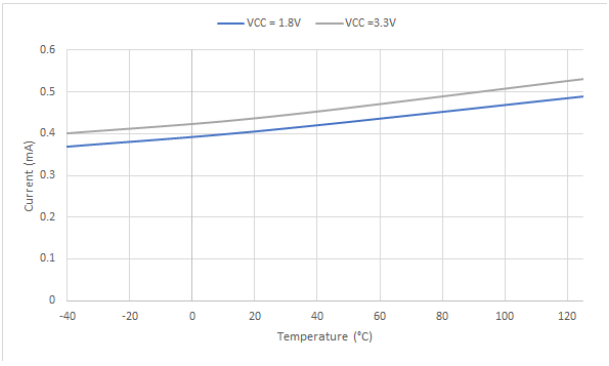

Figure 6-1. Standby Mode ICC vs. Temperature

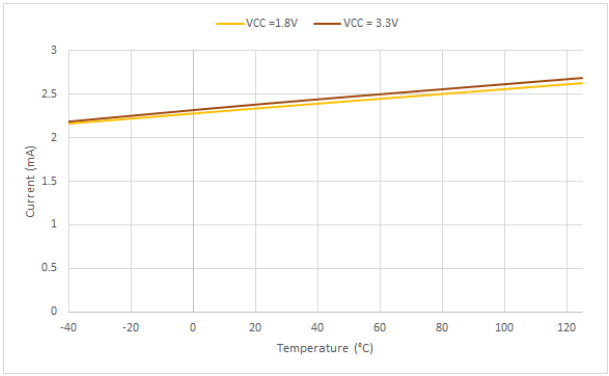

Figure 6-2. Active Mode ICC vs. Temperature

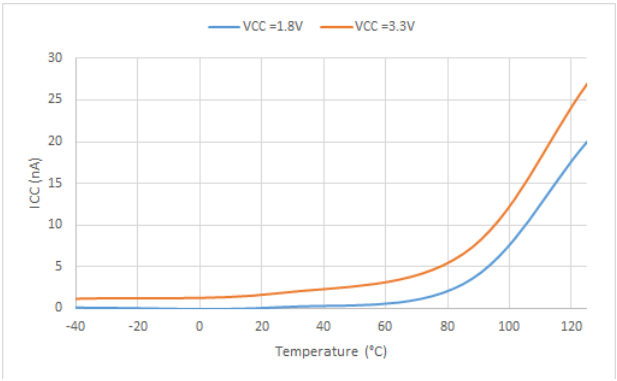

Figure 6-3. Sleep Mode ICC vs. Temperature

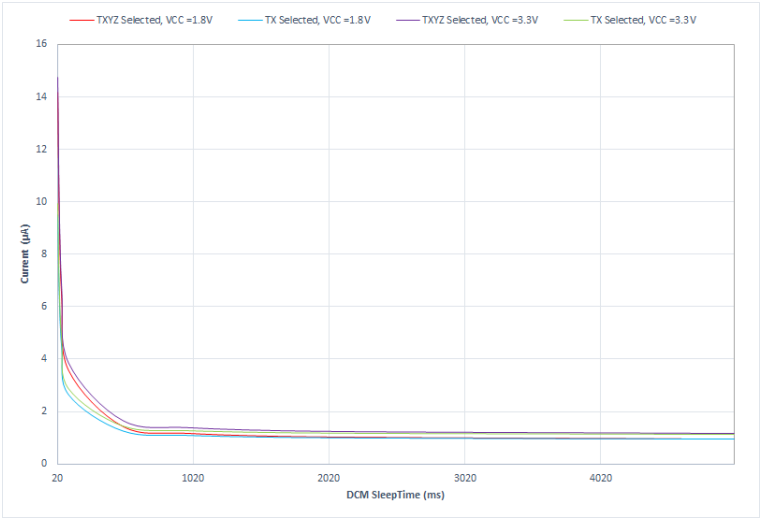

Figure 6-4. Average ICC vs. DCM Mode Sleep Time

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7 Detailed Description

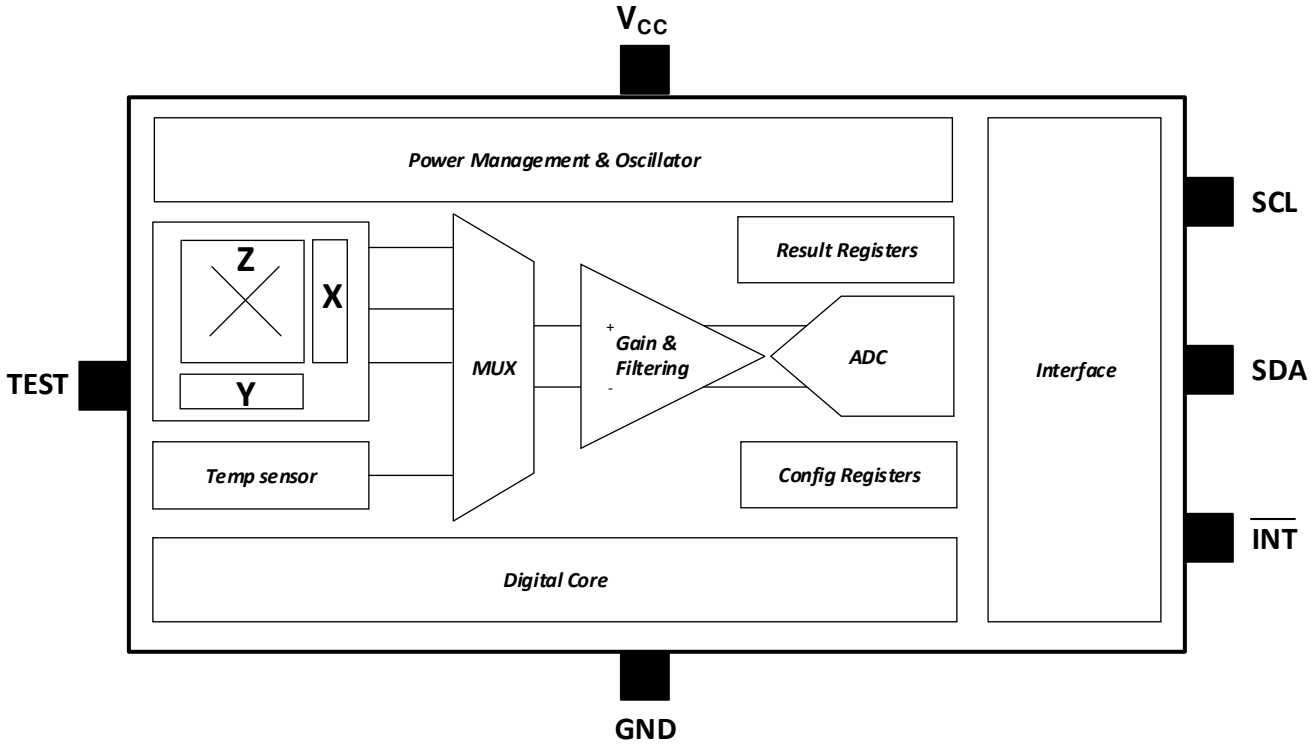
7.1 Overview

The TMAG5273 IC is based on the Hall-effect technology and precision mixed signal circuitry from Texas Instruments. The output signals (raw X, Y, Z magnetic data and temperature data) are accessible through the I^2C interface.

The IC consists of the following functional and building blocks:

- The power mode control system supports two different power rail, the V_{CC}, containing a low-power oscillator, basic biasing, accurate reset, undervoltage detection, and a fast oscillator.
- The sensing and measurement block contains the hall biasing, hall probes with multiplexers, noise filters, temperature sensor, and a 12-bit AD converter. The hall sensor data and temperature data are multiplexed through the same ADC.
- The I^2C interface, containing the register files and I/O pads. The TMAG5273 supports clock speed up to 1MHz at V_{CC} range from 2.3V to 3.6V, and up to 400KHz at V_{CC} range below 2.3V.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Magnetic Flux Direction

As shown in Figure 7-1, the TMAG5273 will generate positive ADC codes in response to a magnetic north pole in the proximity. Similarly, the TMAG5273 will generate negative ADC codes if magnetic south poles approach from the same directions.

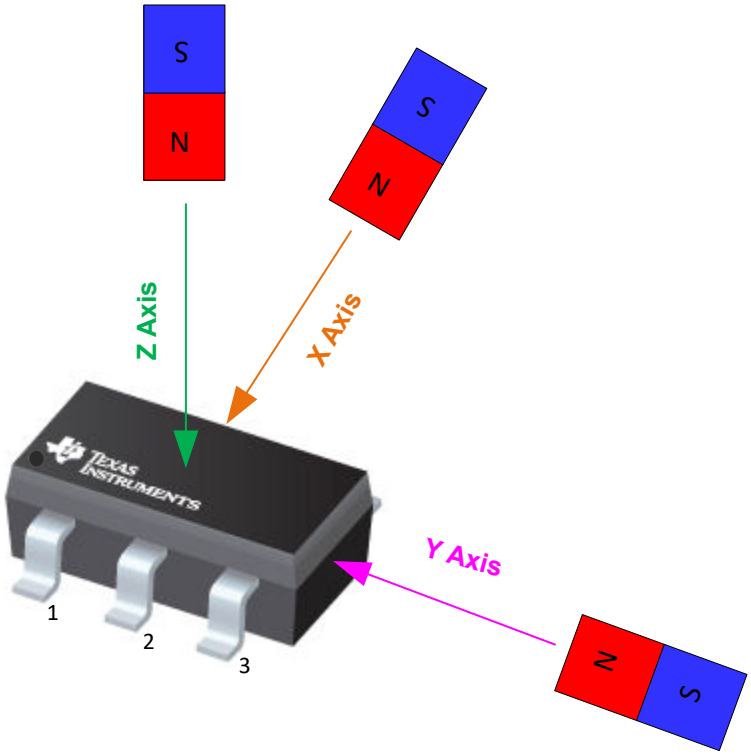


Figure 7-1. Direction of Sensitivity

7.3.2 Sensor Location

Figure 7-2 shows the location of X, Y, Z hall elements inside the TMAG5273.

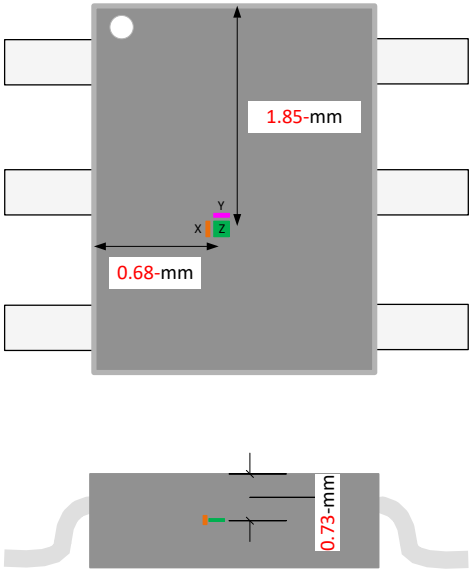


Figure 7-2. Location of X, Y, Z Hall Elements

7.3.3 Interrupt Function

The TMAG5273 supports flexible and configurable interrupt functions through either the $\overline{\text{INT}}$ or the SCL pin. Table 7-1 shows different conversion completion events where result registers and SET_COUNT bits update, and where they do not.

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Table 7-1. Result Register & SET_COUNT Update After Conversion Completion

INT_MODE	Mode Description	I²C Bus Busy, not Talking to Device		I²C Bus Busy & Talking to Device		I²C Bus not Busy	
		Result Update?	SET_COUNT Update?	Result Update?	SET_COUNT Update?	Result Update?	SET_COUNT Update?
000b	No Interrupt	Yes	Yes	No	No	Yes	Yes
001b	Interrupt through $\overline{INT}$	Yes	Yes	No	No	Yes	Yes
010b	Interrupt through $\overline{INT}$Except when I²C Busy	Yes	Yes	No	No	Yes	Yes
011b	Interrupt through SCL	Yes	Yes	No	No	Yes	Yes
100b	Interrupt through SCL Except when I²C Busy	No	No	No	No	Yes	Yes

Note

It is not recommended to share the same I²C bus with multiple secondary devices when using the SCL pin for interrupt function. The SCL interrupt may corrupt transactions with other secondary devices if present in the same I²C bus.

Interrupt Through SCL

Figure 7-3 shows an example for interrupt function through the SCL pin with the device programmed to wake up and measure for threshold cross at a predefined intervals. The wake-up intervals can be set through the SLEEPTIME bits. Once the magnetic threshold cross is detected, the device asserts a fixed width interrupt signal through the SCL pin, and goes back to stand-by mode.

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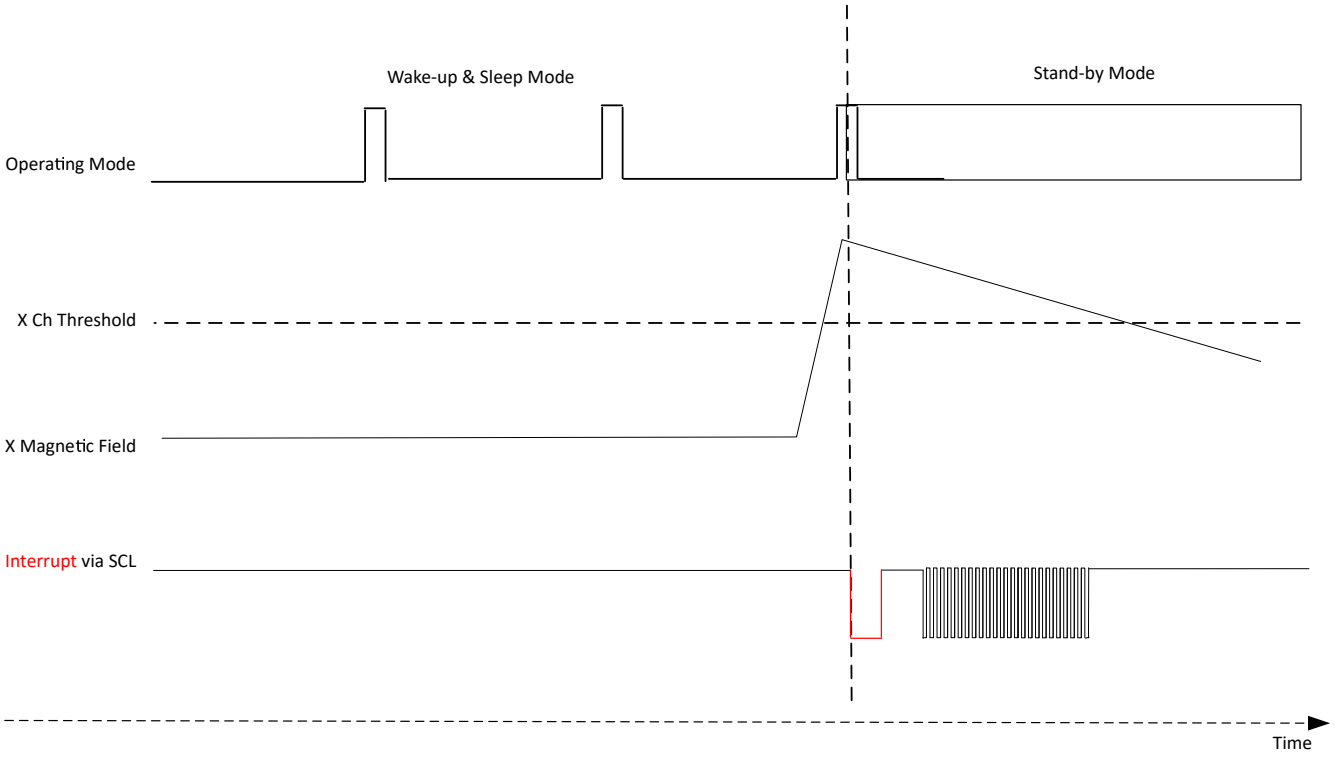

Figure 7-3. Interrupt Through SCL

Fixed Width Interrupt Through $\overline{\text{INT}}$

Figure 7-4 shows an example for fixed-width interrupt function through the $\overline{\text{INT}}$ pin. The device is programmed to be in wake-up & sleep mode to detect a magnetic threshold. The INT_STATE register bit is set 1b. Once the magnetic threshold cross is detected, the device asserts a fixed width interrupt signal through the $\overline{\text{INT}}$ pin, and goes back to stand-by mode.

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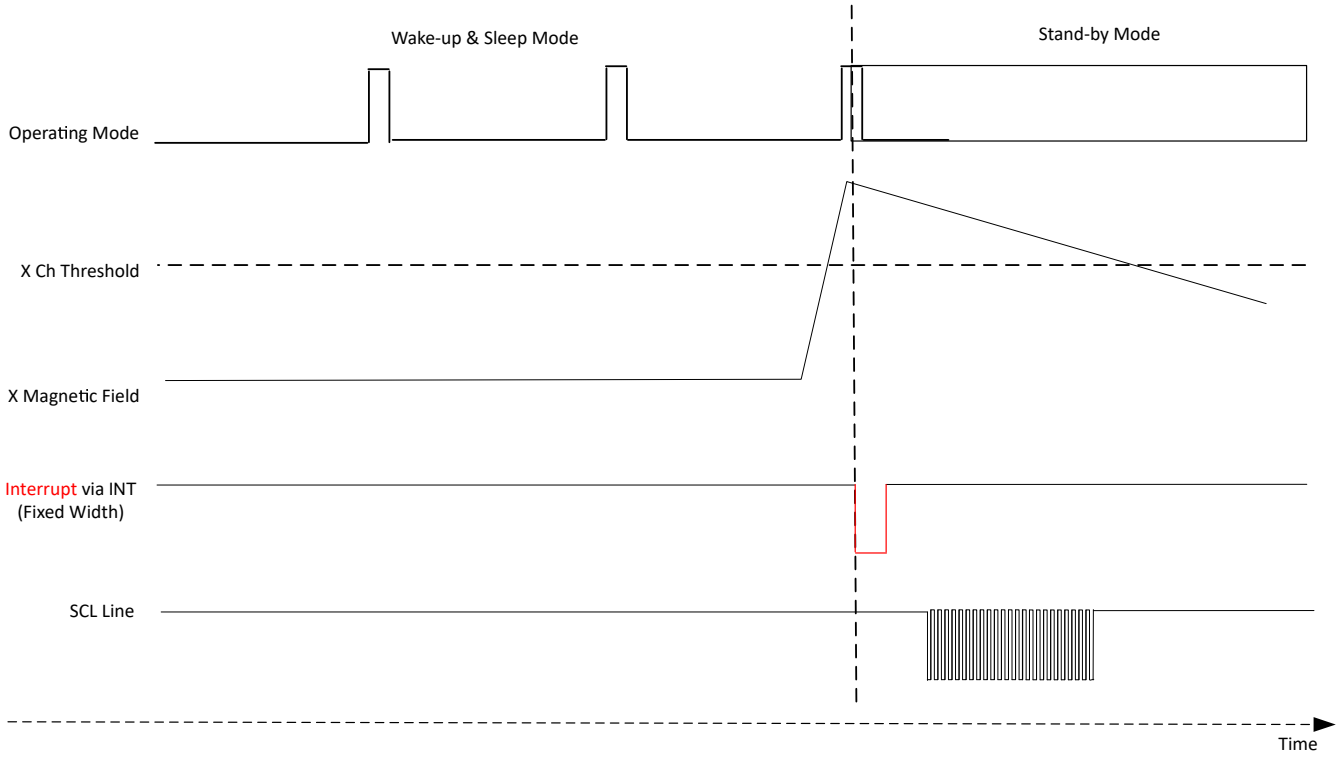

Figure 7-4. Fixed Width Interrupt Through $\overline{\text{INT}}$

Latched Interrupt Through $\overline{\text{INT}}$

Figure 7-5 shows an example for latched interrupt function through the $\overline{\text{INT}}$ pin. The device is programmed to be in wake-up & sleep mode to detect a magnetic threshold. The INT_STATE register bit is set 0b. Once the magnetic threshold cross is detected, the device asserts a latched interrupt signal through the $\overline{\text{INT}}$ pin, and goes back to stand-by mode. The interrupt latch is cleared only after the device receives a valid address through the SCL line.

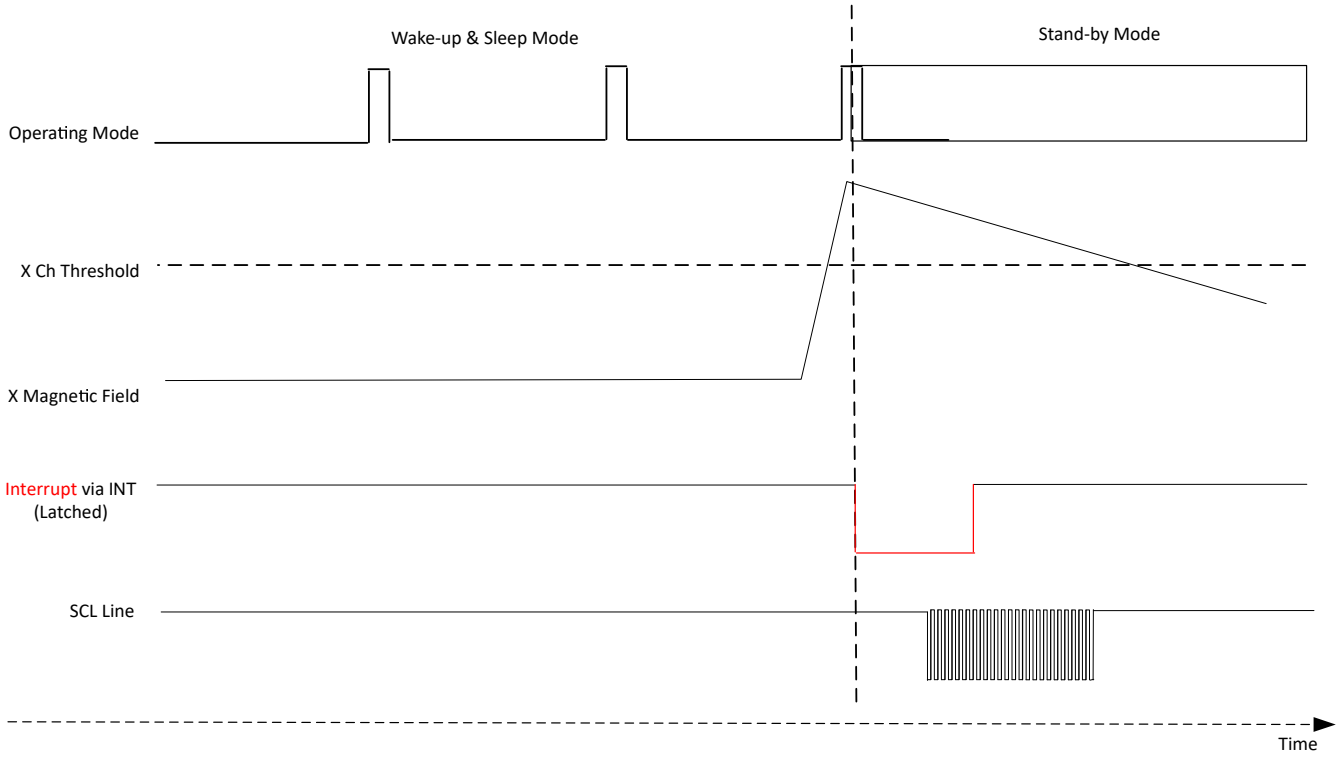

Figure 7-5. Latched Interrupt Through $\overline{\text{INT}}$

7.3.4 Device I²C Address

Table 7-2 shows the default factory programmed I²C addresses of the TMAG5273. The device needs to be addressed with the factory default I²C address after power up. If required, a primary can assign a new I²C address through the I2C_ADDRESS register bits after power up.

Table 7-2. I²C Default Address

Device Version	Magnetic Range	I²C Address (7 MSB Bits)	I²C Write Address (8-Bit)	I²C Read Address (8-Bit)
TMAG5273A1	±40 mT, ±80 mT	35h	6Ah	6Bh
TMAG5273B1		22h	44h	45h
TMAG5273C1		78h	F0h	F1h
TMAG5273D1		44h	88h	89h
TMAG5273A2	±133 mT, ±266 mT	35h	6Ah	6Bh
TMAG5273B2		22h	44h	45h
TMAG5273C2		78h	F0h	F1h
TMAG5273D2		44h	88h	89h

7.3.5 Magnetic Range Selection

Table 7-3 shows the magnetic range selection for the TMAG5273 device. The X, Y, and Z axes range can be selected with the X_Y_RANGE and Z_RANGE register bits.

Table 7-3. Magnetic Range Selection

	RANGE REGISTER SETTING	TMAG5273A1-Q1	TMAG5273A2-Q1	Comment
X, Y Axis Field	X_Y_RANGE = 0b	±40 mT	±133 mT	
	X_Y_RANGE = 1b	±80 mT	±266 mT	Better SNR performance
Z Axis Field	Z_RANGE = 0b	±40 mT	±133 mT	
	Z_RANGE = 1b	±80 mT	±266 mT	Better SNR performance

7.3.6 Update Rate Settings

The TMAG5273 offers multiple update rates to offer design flexibility to system designers. The different update rates can be selected with the CONV_AVG register bits. Table 7-4 shows different update rate settings for the TMAG5273.

Table 7-4. Update Rate Settings

OPERATING MODE	REGISTER SETTING	UPDATE RATE			Comment
		SINGLE AXIS	TWO AXES	THREE AXES	
X, Y, Z Axis	CONV_AVG = 000b	20.0 Ksps	13.3 Ksps	10.0 Ksps	Fastest update rate
X, Y, Z Axis	CONV_AVG = 001b	13.3 Ksps	8.0 Ksps	5.7 Ksps	
X, Y, Z Axis	CONV_AVG = 010b	8.0 Ksps	4.4 Ksps	3.1 Ksps	
X, Y, Z Axis	CONV_AVG = 011b	4.4 Ksps	2.4 Ksps	1.6 Ksps	
X, Y, Z Axis	CONV_AVG = 100b	2.4 Ksps	1.2 Ksps	0.8 Ksps	
X, Y, Z Axis	CONV_AVG = 101b	1.2 Ksps	0.6 Ksps	0.4 Ksps	Best SNR case

7.3.7 Power Saving Modes

The TMAG5273 supports multiple operating modes for wide array of applications as explained in Figure 7-6. A specific operating mode is selected by setting the corresponding value in the OPERATING_MODE register bits. The device starts powering up after VCC supply crosses the minimum threshold as specified in the Recommended Operating Condition (ROC) table.

7.3.7.1 Standby (Trigger) Mode

The TMAG5273 goes to standby mode after first time powering up. At this mode the digital circuitry and oscillators are on, and the device is ready to accept commands from the primary device. Based off the commands the device can start a sensor data conversion, goes to power saving mode, or start data transfer through I^2C interface. A new conversion can be triggered through I^2C command or through $\overline{INT}$ pin. In this mode the device retains the immediate past conversion result data in the corresponding result registers. The time it takes for the device to go to standby mode from power up is denoted by $T_{start\_power\_up}$.

7.3.7.2 Sleep Mode

The TMAG5273 supports an ultra-low power sleep mode where it retains the critical user configuration settings. In this mode the device doesn't retain the conversion result data. A primary can wake up the device from sleep mode through I^2C communications or the $\overline{INT}$ pin. The time it takes for the device to go to stand-by mode from sleep mode is denoted by T_{start_sleep}.

7.3.7.3 Wake-up & Sleep (W&S) Mode

In this mode the TMAG5273 can be configured to go to sleep and wake up at a certain interval, and measure sensor data based off the SLEEPTIME register bits setting. The device can be set to generate an interrupt through the INT_CONFIG_1 register. Once the conversion is complete and the interrupt condition is met, the TMAG5273 will exit the W&S mode and go to the stand-by mode. The last measured data will be stored in the corresponding result registers before the device goes to the stand-by mode. If the interrupt condition isn't met,

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the device will continue to be in the W&S mode to wake up and measure data at the specified interval. A primary can wake up the TMAG5273 anytime during the W&S mode through I²C bus or $\overline{INT}$ pin. The time it takes for the device to go to stand by mode from W&S mode is denoted by T_{start_sleep}.

7.3.7.4 Continuous Measure Mode

In this mode the TMAG5273 continuously measures the sensor data per SENSOR_CONFIG & DEVICE_CONFIG register settings. In this mode the result registers can be accessed through the I2C lines. The time it takes for the device to go from stand-by mode to continuous measure mode is denoted by $T_{start\_measure}$.

7.3.7.5

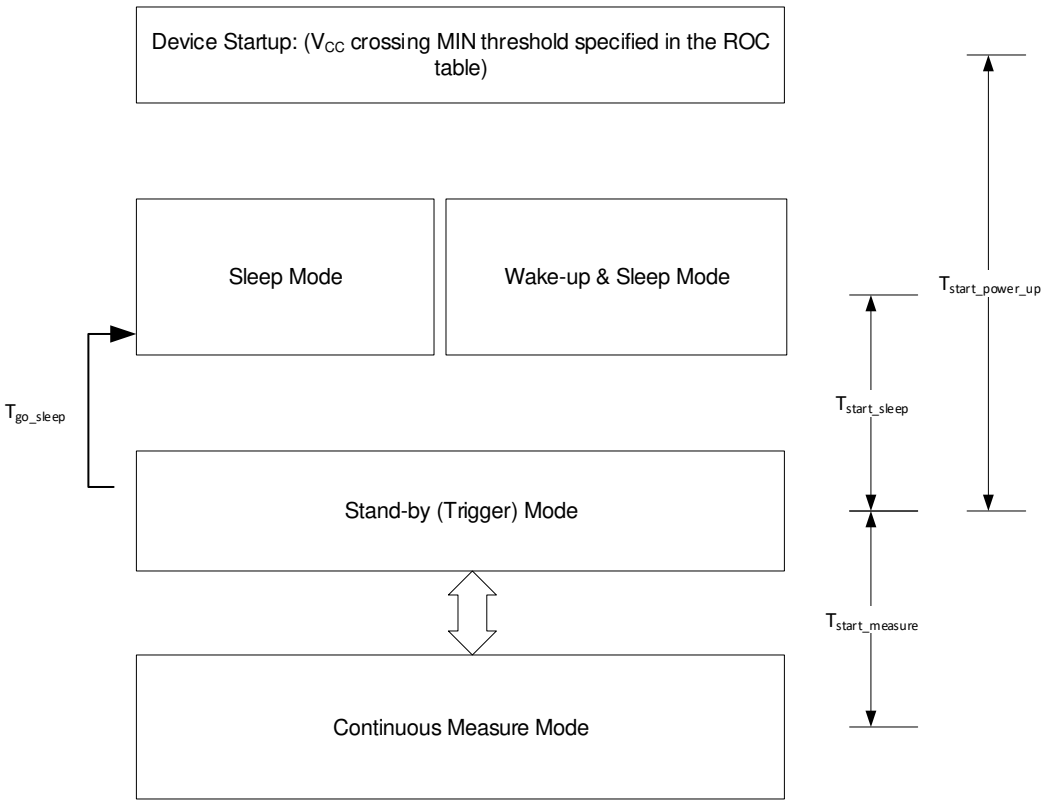

Figure 7-6. TMAG5273 Power-Up Sequence

Table 7-5 shows different device operational modes of the TMAG5273.

Table 7-5. Operating Modes

Operating Mode	Device Function	Access to User Registers	Retain User Configuration	Comment
Continuous Measure Mode	Continuously measuring x, y, z axis, or temperature data	Yes	Yes	
Stand-by Mode	Device is ready to accept I²C commands and start active conversion	Yes	Yes	
Wake-up & Sleep Mode	Wakes up at a certain interval to measure the x, y, z axis, or temperature data	No	Yes	1, 5, 10, 15, 20, 30, 50, 100, 500, 1000, 2000, 5000, & 20000-ms intervals supported.
Sleep Mode	Device retains key configuration settings, but doesn't retain the measurement data	No	Yes	Sleep mode can be utilized by a primary device to implement other power saving intervals not supported by wake-up & sleep mode.

7.4 Programming

7.4.1 I²C Interface

The TMAG5273 offers I²C interface, a two-wire interface to connect low-speed devices like microcontrollers, A/D and D/A converters, I/O interfaces and other similar peripherals in embedded systems.

7.4.1.1 SCL

SCL is the clock line. It is used to synchronize all data transfers over the I²C bus.

7.4.1.2 SDA

SDA is the bidirectional data line for the I²C interface.

7.4.1.3 I²C Read/Write

The TMAG5273 supports multiple I²C read and write frames targeting different applications. I2C_RD and CRC_EN bits offers multiple read frames to optimize the read time, data resolution and data integrity for a select application.

7.4.1.3.1 Standard I²C Write

Figure 7-7 shows an example of standard I²C two byte write command supported by TMAG5273. The starting byte contains 7-bit secondary device address and a '0' at the R/$\overline{W}$ command bit. The MSB of the second byte contains the conversion trigger bit. Writing '1' at this trigger bit will start a new conversion after the register address decoding is completed. The 7 LSB bits of the second byte contains the starting register address for the write command. After the two command bytes, the primary device starts to send the data to be written at the corresponding register address. Each successive write byte will send the data for the successive register address in the secondary device.

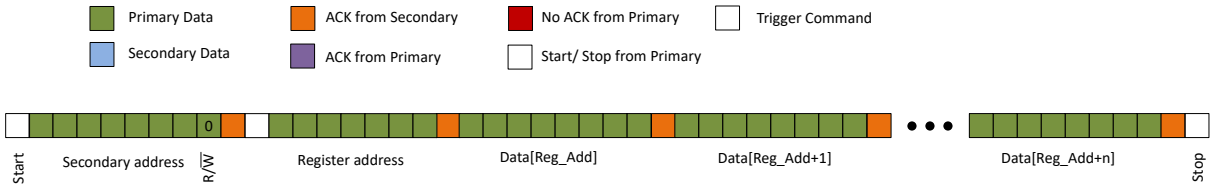

Figure 7-7. Standard I²C Write

7.4.1.3.2 General Call Write

Figure 7-8 shows an example of the general call I²C write command supported by the TMAG5273. This command is useful to configure multiple I²C devices in a I²C bus simultaneously. The starting byte contains 8-bit '0's. The MSB of the second byte contains the conversion trigger bit. Writing '1' at this trigger bit will start a new conversion after the register address decoding is completed. The 7 LSB bits of the second byte contains the starting register address for the write command. After the two command bytes, the primary device starts to send the data to be written at the corresponding register address of all the secondary devices in the I²C bus. Each successive write byte will send the data for the successive register address in the secondary devices.

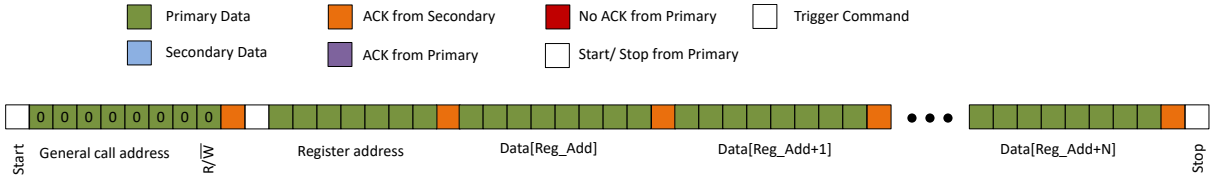

Figure 7-8. General Call I²C Write

7.4.1.3.3 Standard 3-Byte I²C Read

Figure 7-9 and Figure 7-10 show examples of standard I²C three byte read command supported by the TMAG5273. The starting byte contains 7-bit secondary device address and the R/$\overline{W}$ command bit '0'. The MSB of the second byte contains the conversion trigger command bit. Writing '1' at this trigger bit will start a new conversion after the register address decoding is completed. The 7 LSB bits of the second byte contains

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the starting register address for the write command. After receiving ACK signal from secondary, the primary send the secondary address once again with R/$\overline{W}$ command bit as '1'. The secondary starts to send the corresponding register data. It will send successive register data with each successive ACK from primary. If CRC is enabled, the secondary will send the fifth CRC byte based off the CRC calculation of immediate past 4 register bytes.

Note

In the standard 3-byte read command the TMAG5273 doesn't support CRC if the data length is more than 4 byte. Initiate successive read commands for larger data stream requiring CRC.

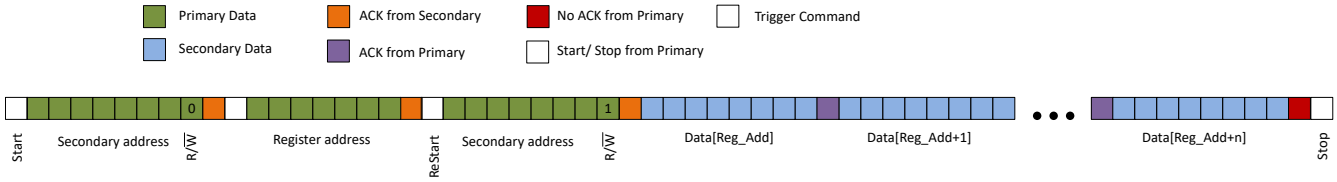

Figure 7-9. Standard 3-Byte I²C Read With CRC Disabled, CRC_EN = 0b

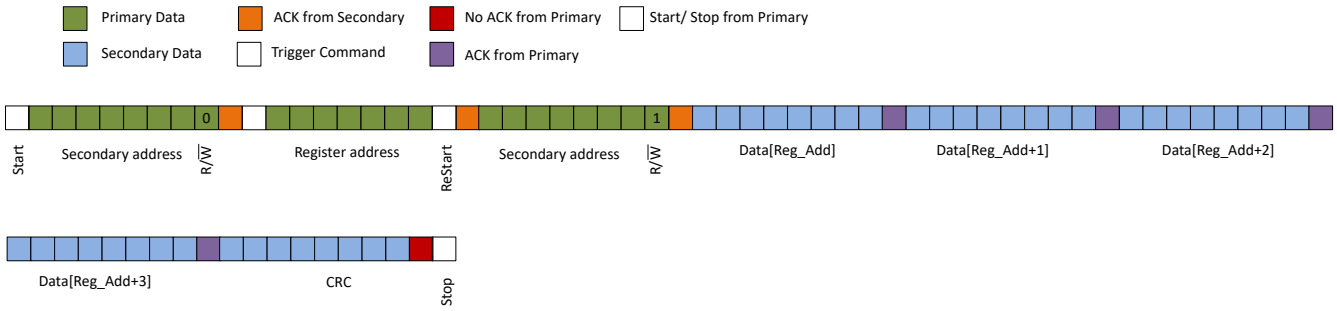

Figure 7-10. Standard 3-Byte I²C Read With CRC Enabled, CRC_EN = 1b

7.4.1.3.4 1-Byte I2C Read Command for 16-Bit Data

Figure 7-11 and Figure 7-12 show examples of 1-byte I²C read command supported by the TMAG5273. Select I2C_RD =01b to enable this mode. The command byte contains 7-bit secondary device address and a '1' at the R/$\overline{W}$ bit. In this mode, per MAG_CH_EN and T_CH_EN bits setting, the device will send 16-bit data of the enabled channels and the CONV_STATUS register data byte. If CRC is enabled, the device will send an additional CRC byte based off the CRC calculation of the command byte and the data sent in the current packet. When multiple channels are enabled, the sent data follows the T, X, Y, and Z sequence in the successive data bytes.

Figure 7-11. 1-Byte I²C Read Command for 16-Bit Data With CRC Disabled, CRC_EN = 0b

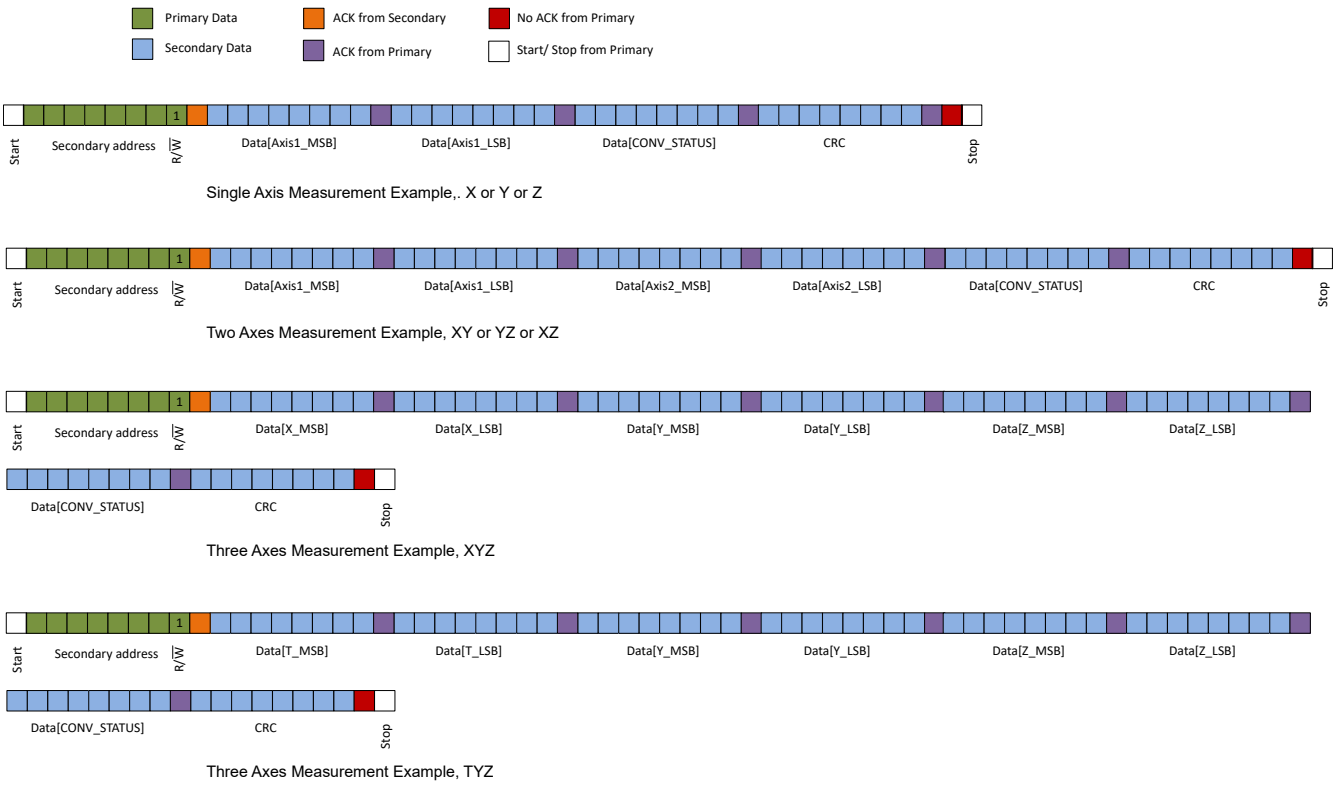

Figure 7-12. 1-Byte I²C Read Command for 16-Bit Data With CRC Enabled, CRC_EN = 1b

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Note

In the 1-byte read command for 16-bit data only up to 3 channels data can be sent when CRC is enabled. This restriction doesn't apply if CRC is disabled.

7.4.1.3.5 1-Byte I²C Read Command for 8-Bit Data

Figure 7-13 and Figure 7-14 show examples of 1-byte I²C read command supported by the TMAG5273. Select I2C_RD =10b to enable this mode. The command byte contains 7-bit secondary device address and a '1' at the R/$\overline{W}$ bit. In this mode, per MAG_CH_EN and T_CH_EN bits setting, the device will send 8-bit data of the enabled channels and the CONV_STATUS register data byte. If CRC is enabled, the device will send an additional CRC byte based off the CRC calculation of the command byte and the data sent in the current packet. When multiple channels are enabled, the sent data follows the T, X, Y, and Z sequence in the successive data bytes.

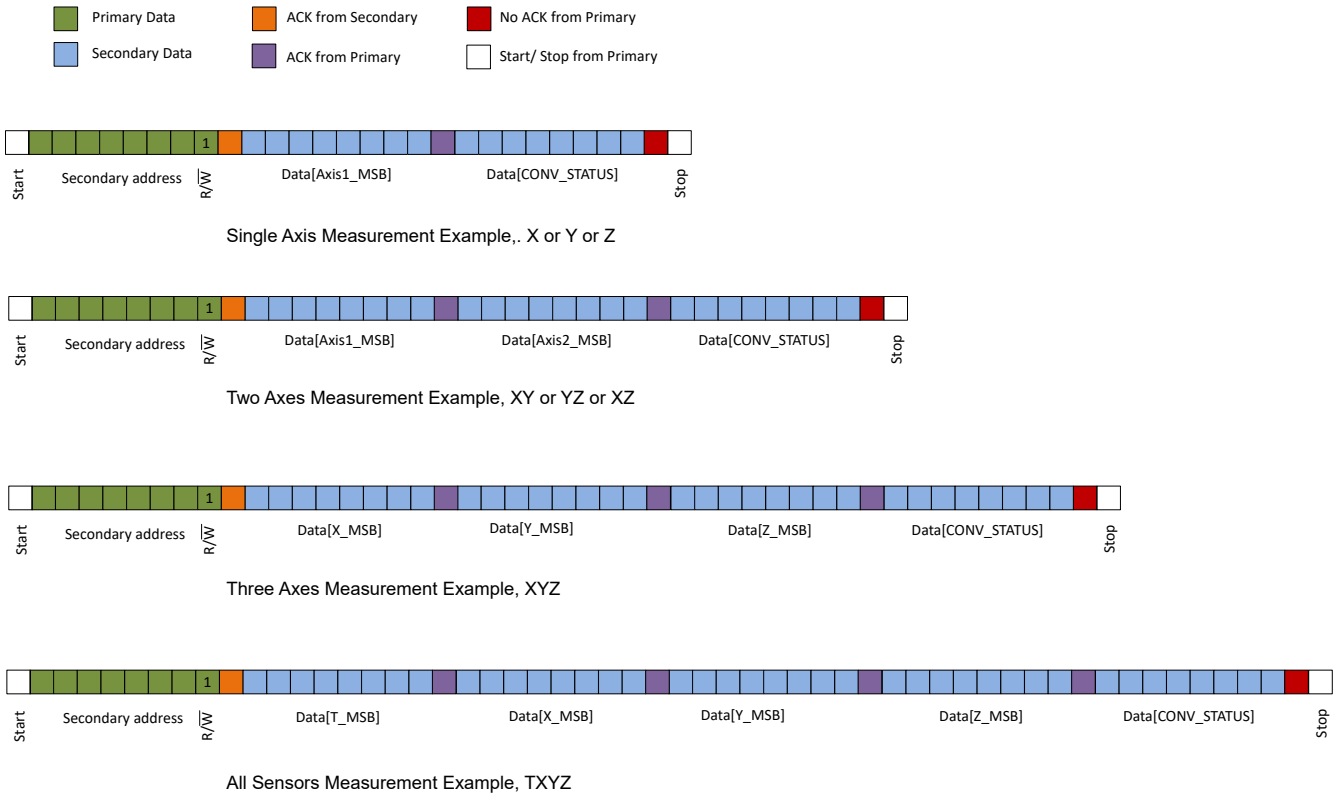

Figure 7-13. 1-Byte I²C Read Command for 8-Bit Data With CRC Disabled, CRC_EN = 0b

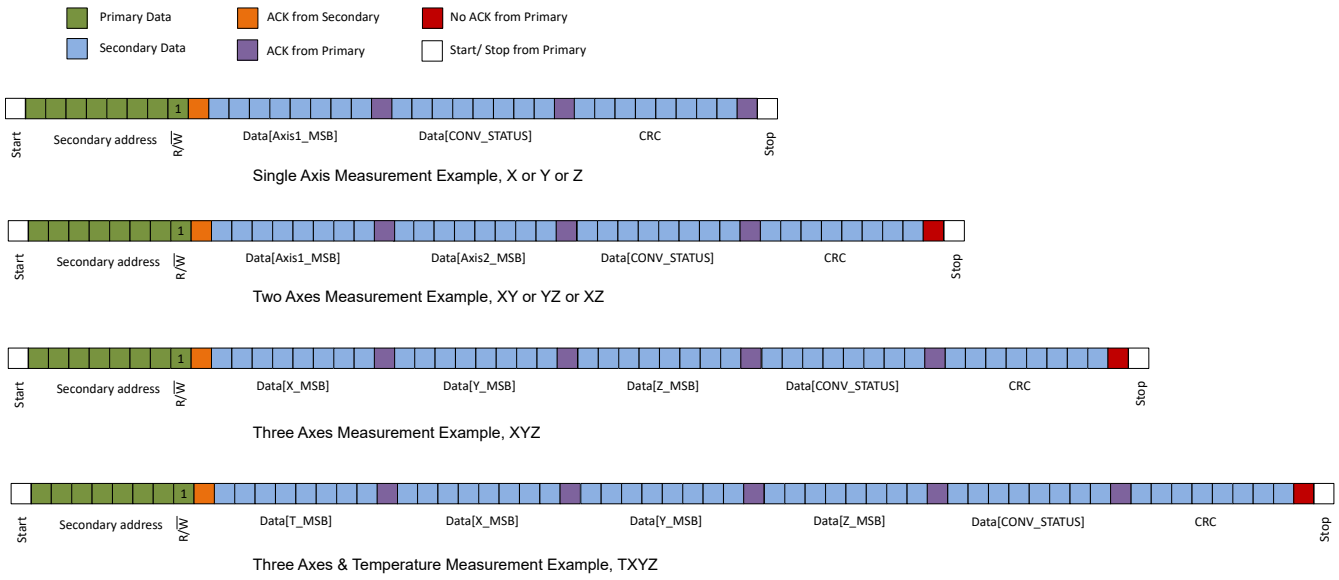

Figure 7-14. 1-Byte I²C Read Command for 8-Bit Data With CRC Enabled, CRC_EN = 1b

Note

In the 1-byte read command for 8-bit data any combinations of channels can be sent without restrictions.

7.4.1.3.6 I²C Read CRC

The TMAG5273 supports optional CRC during I²C read. The CRC can be enabled through the CRC_EN register bit. The CRC is performed on a data string that is determined by the I²C read type. The CRC information is sent as a single byte after the data bytes. The code is generated by the polynomial $x^8 + x^2 + x + 1$. Initial CRC bits are FFh.

The following equations can be employed to calculate CRC:

d = Data Input, c = Initial CRC (FFh) (1)

newcrc[0] = d[7] ^ d[6] ^ d[0] ^ c[0] ^ c[6] ^ c[7] (2)

newcrc[1] = d[6] ^ d[1] ^ d[0] ^ c[0] ^ c[1] ^ c[6] (3)

newcrc[2] = d[6] ^ d[2] ^ d[1] ^ d[0] ^ c[0] ^ c[1] ^ c[2] ^ c[6] (4)

newcrc[3] = d[7] ^ d[3] ^ d[2] ^ d[1] ^ c[1] ^ c[2] ^ c[3] ^ c[7] (5)

newcrc[4] = d[4] ^ d[3] ^ d[2] ^ c[2] ^ c[3] ^ c[4] (6)

newcrc[5] = d[5] ^ d[4] ^ d[3] ^ c[3] ^ c[4] ^ c[5] (7)

newcrc[6] = d[6] ^ d[5] ^ d[4] ^ c[4] ^ c[5] ^ c[6] (8)

newcrc[7] = d[7] ^ d[6] ^ d[5] ^ c[5] ^ c[6] ^ c[7] (9)

The following examples show calculated CRC byte based off various input data:

I2C Data 00h : CRC = F3h

I2C Data FFh : CRC = 00h

I2C Data 80h : CRC = 7Ah

I2C Data 4Ch : CRC = 10h

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I2C Data E0h : CRC = 5Dh

I2C Data 00000000h : CRC = D1h

I2C Data FFFFFFFFh : CRC = 0Fh

7.4.2 Data Definition

7.4.2.1 Magnetic Sensor Data

The X, Y, and Z magnetic sensor data are stored in x_MSB_RESULT and x_LSB_RESULT registers. Each sensor output is stored in 16-bit 2's complement format in two 8-bit registers as shown in Figure 7-15. The data can be retrieved as 16-bit format combining both MSB and LSB registers, or as 8-bit format through the MSB register.

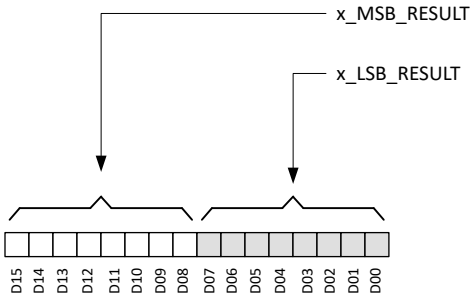

Figure 7-15. Magnetic Sensor Data Definition

The measured magnetic field can be calculated using Equation 10 for 16-bit data, and using Equation 11 for 8-bit data.

$$B = \frac{-(D_{15} \times 2^{15}) + \sum_{i=0}^{14} D_i \times 2^i}{2^{16}} \times 2|B_R| \quad (10)$$

where

- B is magnetic field in mT.
- D_i is the data bit as shown in Figure 7-15.
- B_R is the magnetic range in mT for the corresponding channel.

$$B = \frac{-(D_{15} \times 2^{7}) + \sum_{i=0}^{6} D_{i+8} \times 2^i}{2^{8}} \times 2|B_R| \quad (11)$$

7.4.2.2 Temperature Sensor Data

The TMAG5273 will measure temperature from –40 °C to 170 °C. The temperature sensor data are stored in T_MSB_RESULT and T_LSB_RESULT registers. The sensor output is stored in 16-bit 2's complement format in two 8-bit registers as shown in Figure 7-16. The data can be retrieved as 16-bit format combining both MSB and LSB registers, or as 8-bit format through the MSB register.

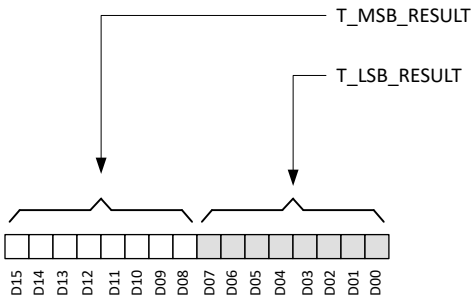

Figure 7-16. Temperature Sensor Data Definition

The measured temperature in degree Celsius can be calculated using Equation 12 for 16-bit data, and using Equation 13 for 8-bit data.

$$T = T_{SENS\_T0} + \frac{T_{ADC\_T} - T_{ADC\_T0}}{T_{ADC\_RES}} \tag{12}$$

where

- T is the measured temperature in degree Celsius.
- T_{SENS_T0} as listed in the *Electrical Characteristics* table.
- T_{ADC_RES} is the change in ADC code per degree Celsius.
- T_{ADC_T0} as listed in the *Electrical Characteristics* table.
- T_{ADC_T} is the measured ADC code for temperature T.

$$T = T_{SENS\_T0} + \frac{256 \times \left(T_{ADC\_T} - \frac{T_{ADC\_T0}}{256}\right)}{T_{ADC\_RES}} \tag{13}$$

7.4.2.3 Angle and Magnitude Data Definition

The TMAG5273 calculates the angle from a pair of magnetic axes based off the ANGLE_EN register bits setting. The ANGLE_RESULT_MSB and ANGLE_RESULT_LSB registers store the angle information as shown in Figure 7-17. Bits D04-D12 store angle integer value from 0 to 360 degree. Bits D00-D03 store fractional angle value. The 3-MSB bits are always populated as b000. The angle can be calculated using Equation 14.

$$A = \sum_{i=4}^{12} D_i \times 2^{i-4} + \frac{\sum_{i=0}^{3} D_i \times 2^i}{16} \tag{14}$$

where

- A is the angle measured in degree.
- D_i is the data bit as shown in Figure 7-17.

For example: a 354.50 degree is populated as 0001 0110 0010 1000b and a 17.25 degree is populated as 000 0001 0001 0100b.

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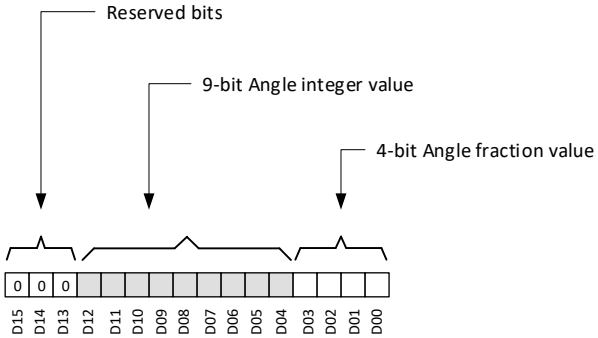

Figure 7-17. Angle Data Definition

During the angle calculation, use Equation 15 to calculate the resultant vector magnitude.

$$M = \sqrt{MADC_{Ch1}{}^2 + MADC_{Ch2}{}^2} \tag{15}$$

where

- $MADC_{Ch1}$, $MADC_{Ch2}$ are the ADC codes of the two magnetic channels selected for the angle calculation.

The magnitude value is stored in the MAGNITUDE_RESULT register as shown in Magnitude Result Data Definition. For on-axis angular measurement the magnitude value should remain constant across the full 360° measurement.

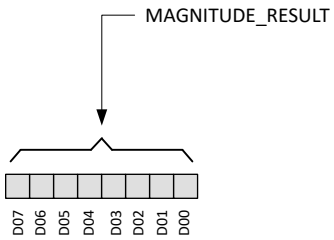

Figure 7-18. Magnitude Result Data Definition

7.4.2.4 Magnetic Sensor Offset Correction

The TMAG5273 enables offset correction of a pair of magnetic axes as shown in Figure 7-19. The MAG_OFFSET_CONFIG_1 and MAG_OFFSET_CONFIG_2 registers store the offset values to be corrected in 2's complement data format. The selection and order of the sensors are defined in the ANGLE_EN register bits setting. The default value of these offset correction registers are set as zero.

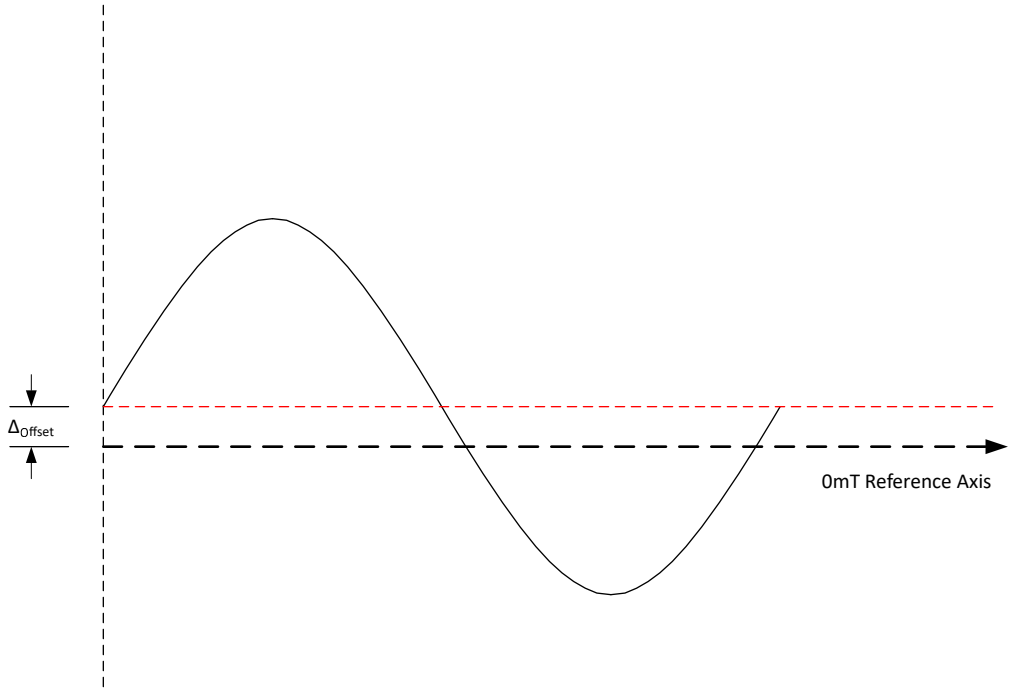

Figure 7-19. Magnetic Sensor Data Offset Correction

The amount of offset for each axis can be calculated using Equation 16. As an example, with a ±40mT range, MAG_OFFSET_CONFIG_1 set at 10000000b, and MAG_OFFSET_CONFIG_2 set at 0001000b, the offset correction for the first axis is −2.5mT and second axis is 0.312mT.

$$\Delta_{Offset} = \frac{-(D_7 \times 2^7) + \sum_{i=0}^{6} D_i \times 2^i}{2^{12}} \times 2|B_R| \quad (16)$$

where

- Δ_{Offset} is the amount of offset correction to be applied in mT.
- D_i is the data bit in the offset MAG_OFFSET_CONFIG_x register.
- B_R is the magnetic range in mT for the corresponding channel.

7.5 Register Map

7.5.1 TMAG5273 Registers

Table 7-6 lists the TMAG5273 registers. All register offset addresses not listed in Table 7-6 should be considered as reserved locations and the register contents should not be modified.

User Configuration Registers

Table 7-6. TMAG5273 Registers

Offset	Acronym	Register Name	Section
0h	DEVICE_CONFIG_1	Configure Device Operation Modes	Go
1h	DEVICE_CONFIG_2	Configure Device Operation Modes	Go
2h	SENSOR_CONFIG_1	Sensor Device Operation Modes	Go
3h	SENSOR_CONFIG_2	Sensor Device Operation Modes	Go
4h	X_THR_CONFIG	X Threshold Configuration	Go
5h	Y_THR_CONFIG	Y Threshold Configuration	Go
6h	Z_THR_CONFIG	Z Threshold Configuration	Go

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Table 7-6. TMAG5273 Registers (continued)

Offset	Acronym	Register Name	Section
7h	T_CONFIG	Temp Sensor Configuration	Go
8h	INT_CONFIG_1	Configure Device Operation Modes	Go
9h	MAG_GAIN_CONFIG	Configure Device Operation Modes	Go
Ah	MAG_OFFSET_CONFIG_1	Configure Device Operation Modes	Go
Bh	MAG_OFFSET_CONFIG_2	Configure Device Operation Modes	Go
Ch	I2C_ADDRESS	I^2C Address Register	Go
Dh	DEVICE_ID	ID for the device die	Go
Eh	MANUFACTURER_ID_LSB	Manufacturer ID lower byte	Go
Fh	MANUFACTURER_ID_MSB	Manufacturer ID upper byte	Go
10h	T_MSB_RESULT	Conversion Result Register	Go
11h	T_LSB_RESULT	Conversion Result Register	Go
12h	X_MSB_RESULT	Conversion Result Register	Go
13h	X_LSB_RESULT	Conversion Result Register	Go
14h	Y_MSB_RESULT	Conversion Result Register	Go
15h	Y_LSB_RESULT	Conversion Result Register	Go
16h	Z_MSB_RESULT	Conversion Result Register	Go
17h	Z_LSB_RESULT	Conversion Result Register	Go
18h	CONV_STATUS	Conversion Status Register	Go
19h	ANGLE_RESULT_MSB	Conversion Result Register	Go
1Ah	ANGLE_RESULT_LSB	Conversion Result Register	Go
1Bh	MAGNITUDE_RESULT	Conversion Result Register	Go
1Ch	DEVICE_STATUS	Device_Diag Status Register	Go

Complex bit access types are encoded to fit into small table cells. Table 7-7 shows the codes that are used for access types in this section.

Table 7-7. TMAG5273 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1CP	W 1C P	Write 1 to clear Requires privileged access
Reset or Default Value		
- *n*		Value after reset or the default value

7.5.1.1 DEVICE_CONFIG_1 Register (Offset = 0h) [Reset = 0h]

DEVICE_CONFIG_1 is shown in Table 7-8.

Return to the Summary Table.

Table 7-8. DEVICE_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CRC_EN	R/W	0h	Enables I2C CRC byte to be sent 0h = CRC disabled 1h = CRC enabled

Table 7-8. DEVICE_CONFIG_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-5	MAG_TEMPCO	R/W	0h	Temperature coefficient of the magnet 0h = 0% (No temperature compensation) 1h = 0.12%/ deg C (NdBFe) 2h = Reserved 3h = 0.2%/deg C (Ceramic)
4-2	CONV_AVG	R/W	0h	Enables additional sampling of the sensor data to reduce the noise effect (or to increase resolution) 0h = 1x - 10.0Ksps (3-axes) or 20Ksps (1 axis) 1h = 2x - 5.7Ksps (3-axes) or 13.3Ksps (1 axis) 2h = 4x - 3.1Ksps (3-axes) or 8.0Ksps (1 axis) 3h = 8x - 1.6Ksps (3-axes) or 4.4Ksps (1 axis) 4h = 16x - 0.8Ksps (3-axes) or 2.4Ksps (1 axis) 5h = 32x - 0.4Ksps (3-axes) or 1.2Ksps (1 axis)
1-0	I2C_RD	R/W	0h	Defines the I^2C read mode 0h = Standard I^2C 3-byte read command 1h = 1-byte I^2C read command for 16-bit sensor data and conversion status 2h = 1-byte I^2C read command for 8-bit sensor MSB data and conversion status 3h = Reserved

7.5.1.2 DEVICE_CONFIG_2 Register (Offset = 1h) [Reset = 0h]

DEVICE_CONFIG_2 is shown in Table 7-9.

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Table 7-9. DEVICE_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	THR_HYST	R/W	0h	Select thresholds for the interrupt function 0h = Takes the 2's complement value of each x_THR_CONFIG register to create a magnetic threshold of the corresponding axis 1h = Takes the 7 LSB bits of the x_THR_CONFIG register to create two opposite magnetic thresholds (one north, and another south) of equal magnitude. 2h = Reserved 3h = Reserved 4h = Reserved 5h = Reserved 6h = Reserved 7h = Reserved
4	LP_LN	R/W	0h	Selects the modes between low active current or low-noise modes 0h = Low active current mode 1h = Low noise mode
3	I2C_GLITCH_FILTER	R/W	0h	I^2C glitch filter 0h = Glitch filter on 1h = Glitch filter off
2	TRIGGER_MODE	R/W	0h	Selects a condition which initiates a single conversion based off already configured registers. A running conversion completes before executing a trigger. Redundant triggers are ignored. TRIGGER_MODE is available only during the modes explicitly mentioned in OPERATING_MODE. 0h = Conversion Start at I^2C Command Bits, DEFAULT 1h = Conversion starts through trigger signal at $\overline{INT}$ pin

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Table 7-9. DEVICE_CONFIG_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	OPERATING_MODE	R/W	0h	Selects Operating Mode and updates value based on operating mode if device transitions from Wake-up and sleep mode to Standby mode. 0h = Standby Mode (starts new conversion at trigger event) 1h = Sleep mode 2h = Continuous mode 3h = Wake-up and Sleep mode (duty-cycled mode)

7.5.1.3 SENSOR_CONFIG_1 Register (Offset = 2h) [Reset = 0h]

SENSOR_CONFIG_1 is shown in Table 7-10.

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Table 7-10. SENSOR_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	MAG_CH_EN	R/W	0h	Enables data acquisition of the magnetic axis channel(s) 0h = All magnetic channels of off, DEFAULT 1h = X channel enabled 2h = Y channel enabled 3h = X, Y channel enabled 4h = Z channel enabled 5h = Z, X channel enabled 6h = Y, Z channel enabled 7h = X, Y, Z channel enabled 8h = XYX channel enabled 9h = YXY channel enabled Ah = YZY channel enabled Bh = XZX channel enabled Ch = Reserved Dh = Reserved Eh = Reserved Fh = Reserved
3-0	SLEEPTIME	R/W	0h	Selects the time spent in low power mode between conversions when OPERATING_MODE =11b 0h = 1ms 1h = 5ms 2h = 10ms 3h = 15ms 4h = 20ms 5h = 30ms 6h = 50ms 7h = 100ms 8h = 500ms 9h = 1000ms Ah = 2000ms Bh = 5000ms Ch = 20000ms

7.5.1.4 SENSOR_CONFIG_2 Register (Offset = 3h) [Reset = 0h]

SENSOR_CONFIG_2 is shown in Table 7-11.

Return to the Summary Table.

Table 7-11. SENSOR_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved

Table 7-11. SENSOR_CONFIG_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	THRX_COUNT	R/W	0h	Number of threshold crossings before the interrupt is assereted 0h = 1 threshold crossing 1h = 4 threshold crossing
5	MAG_THR_DIR	R/W	0h	Selects the direction of threshold check. This bit is ignored when THR_HYST > 001b 0h = sets interrupt for field above the threshold 1h = sets interrupt for field below the threshold
4	MAG_GAIN_CH	R/W	0h	Selects the axis for magnitude gain correction value entered in MAG_GAIN_CONFIG register 0h = 1st channel is selected for gain adjustment 1h = 2nd channel is selected for gain adjustment
3-2	ANGLE_EN	R/W	0h	Enables angle calculation, magnetic gain, and offset corrections between two selected magnetic channels 0h = No angle calculation, magnitude gain, and offset correction enabled 1h = X 1st, Y 2nd 2h = Y 1st, Z 2nd 3h = X 1st, Z 2nd
1	X_Y_RANGE	R/W	0h	Select the X and Y axes magnetic range from 2 different options. 0h = ±40mT (TMAG5273A1) or ±133mT (TMAG5273A2), DEFAULT 1h = ±80mT (TMAG5273A1) or ±266mT (TMAG5273A2)
0	Z_RANGE	R/W	0h	Select the Z axis magnetic range from 2 different options. 0h = ±40mT (TMAG5273A1) or ±133mT (TMAG5273A2), DEFAULT 1h = ±80mT (TMAG5273A1) or ±266mT (TMAG5273A2)

7.5.1.5 X_THR_CONFIG Register (Offset = 4h) [Reset = 0h]

X_THR_CONFIG is shown in Table 7-12.

Return to the Summary Table.

Table 7-12. X_THR_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	X_THR_CONFIG	R/W	0h	8-bit, 2' complement X axis threshold code for limit check. The range of possible threshold entrees can be +/-128. The threshold value in mT is calculated for A1 as (40(1+X_Y_RANGE)/128)*X_THR_CONFIG, for A2 as (133(1+X_Y_RANGE)/128)*X_THR_CONFIG. Default 0h means no threshold comparison.

7.5.1.6 Y_THR_CONFIG Register (Offset = 5h) [Reset = 0h]

Y_THR_CONFIG is shown in Table 7-13.

Return to the Summary Table.

Table 7-13. Y_THR_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Y_THR_CONFIG	R/W	0h	8-bit, 2' complement Y axis threshold code for limit check. The range of possible threshold entrees can be +/-128. The threshold value in mT is calculated for A1 as (40(1+X_Y_RANGE)/128)*X_THR_CONFIG, for A2 as (133(1+X_Y_RANGE)/128)*X_THR_CONFIG. Default 0h means no threshold comparison.

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7.5.1.7 Z_THR_CONFIG Register (Offset = 6h) [Reset = 0h]

Z_THR_CONFIG is shown in Table 7-14.

Return to the Summary Table.

Table 7-14. Z_THR_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Z_THR_CONFIG	R/W	0h	8-bit, 2' complement Z axis threshold code for limit check. The range of possible threshold entrees can be +/-128. The threshold value in mT is calculated for A1 as (40(1+Z_RANGE)/128)*Z_THR_CONFIG, for A2 as (133(1+Z_RANGE)/128)*Z_THR_CONFIG. Default 0h means no threshold comparison.

7.5.1.8 T_CONFIG Register (Offset = 7h) [Reset = 0h]

T_CONFIG is shown in Table 7-15.

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Table 7-15. T_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	T_THR_CONFIG	R/W	0h	Temperature threshold code entered by user. The valid temperature threshold ranges are -41C to 170C with the threshold codes for -41C = 1Ah, and 170C = 34h. Resolution is 8 degree C/ LSB. Default 0h means no threshold comparison.
0	T_CH_EN	R/W	0h	Enables data acquisition of the temperature channel 0h = Temp channel disabled 1h = Temp channel enabled

7.5.1.9 INT_CONFIG_1 Register (Offset = 8h) [Reset = 0h]

INT_CONFIG_1 is shown in Table 7-16.

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Table 7-16. INT_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSLT_INT	R/W	0h	Enable interrupt response on conversion complete. 0h = Interrupt is not asserted when the configured set of conversions are complete 1h = Interrupt is asserted when the configured set of conversions are complete
6	THRSLD_INT	R/W	0h	Enable interrupt response on a predefined threshold cross. 0h = Interrupt is not asserted when a threshold is crossed 1h = Interrupt is asserted when a threshold is crossed
5	INT_STATE	R/W	0h	$\overline{\text{INT}}$ interrupt latched or pulsed. 0h = $\overline{\text{INT}}$ interrupt latched until clear by a primary addressing the device 1h = $\overline{\text{INT}}$ interrupt pulse for 10us
4-2	INT_MODE	R/W	0h	Interrupt mode select. 0h = No interrupt 1h = Interrupt through $\overline{\text{INT}}$ 2h = Interrupt through $\overline{\text{INT}}$ except when I^2C bus is busy. 3h = Interrupt through SCL 4h = Interrupt through SCL except when I^2C bus is busy. 5h = Reserved 6h = Reserved 7h = Reserved
1	RESERVED	R	0h	Reserved

Table 7-16. INT_CONFIG_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MASK_INTB	R/W	0h	Mask $\overline{INT}$ pin when $\overline{INT}$ connected to GND 0h = $\overline{INT}$ pin is enabled 1h = $\overline{INT}$ pin is disabled (for wake-up and trigger functions)

7.5.1.10 MAG_GAIN_CONFIG Register (Offset = 9h) [Reset = 0h]

MAG_GAIN_CONFIG is shown in Table 7-17.

Return to the Summary Table.

Table 7-17. MAG_GAIN_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GAIN_VALUE	R/W	0h	8-bit gain value determined by a primary to adjust a Hall axis gain. The particular axis is selected based off the settings of MAG_GAIN_CH and ANGLE_EN register bits. The binary 8-bit input is interpreted as a fractional value in between 0 and 1 based off the formula, 'user entered value in decimal/256'. Gain value of 0 is interpreted by the device as 1.

7.5.1.11 MAG_OFFSET_CONFIG_1 Register (Offset = Ah) [Reset = 0h]

MAG_OFFSET_CONFIG_1 is shown in Table 7-18.

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Table 7-18. MAG_OFFSET_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OFFSET_VALUE_1ST	R/W	0h	8-bit, 2s complement offset value determined by a primary to adjust first axis offset value. The range of possible offset valid entrees can be +/-128. The offset value is calculated by multiplying bit resolution with the entered value.

7.5.1.12 MAG_OFFSET_CONFIG_2 Register (Offset = Bh) [Reset = 0h]

MAG_OFFSET_CONFIG_2 is shown in Table 7-19.

Return to the Summary Table.

Table 7-19. MAG_OFFSET_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OFFSET_VALUE_2ND	R/W	0h	8-bit, 2s complement offset value determined by a primary to adjust second axis offset value. The range of possible offset valid entrees can be +/-128. The offset value is calculated by multiplying bit resolution with the entered value.

7.5.1.13 I2C_ADDRESS Register (Offset = Ch) [Reset = 6Ah]

I2C_ADDRESS is shown in Table 7-20.

Return to the Summary Table.

Table 7-20. I2C_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	I2C_ADDRESS	R/W	35h	7-bit default factory I^2C address is loaded from OTP during first power up. Change these bits to a new setting if a new I^2C address is required (at each power cycle these bits need to be written again to avoid going back to default factory address).

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Table 7-20. I2C_ADDRESS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	I2C_ADDRESS_UPDATE_EN	R/W	0h	Enable a new user defined I^2C address. 0h = Disable update of I2C address 1h = Enable update of I^2C address with bits (7:1)

7.5.1.14 DEVICE_ID Register (Offset = Dh) [Reset = 12h]

DEVICE_ID is shown in Table 7-21.

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Table 7-21. DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	4h	Reserved
1-0	VER	R	2h	Device version indicator. 0h = Reserved 1h = TMAG5273 A1 unit 2h = TMAG5273 A2 unit 3h = Reserved

7.5.1.15 MANUFACTURER_ID_LSB Register (Offset = Eh) [Reset = 49h]

MANUFACTURER_ID_LSB is shown in Table 7-22.

Return to the Summary Table.

Table 7-22. MANUFACTURER_ID_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MANUFACTURER_ID_[7:0]	R	49h	8-bit unique manufacturer ID

7.5.1.16 MANUFACTURER_ID_MSB Register (Offset = Fh) [Reset = 54h]

MANUFACTURER_ID_MSB is shown in Table 7-23.

Return to the Summary Table.

Table 7-23. MANUFACTURER_ID_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MANUFACTURER_ID_[15:8]	R	54h	8-bit unique manufacturer ID

7.5.1.17 T_MSB_RESULT Register (Offset = 10h) [Reset = 0h]

T_MSB_RESULT is shown in Table 7-24.

Return to the Summary Table.

Table 7-24. T_MSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	T_CH_RESULT [15:8]	R	0h	T-channel data conversion results, MSB 8 bits.

7.5.1.18 T_LSB_RESULT Register (Offset = 11h) [Reset = 0h]

T_LSB_RESULT is shown in Table 7-25.

Return to the Summary Table.

Table 7-25. T_LSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	T_CH_RESULT [7:0]	R	0h	T-channel data conversion results, LSB 8 bits.

7.5.1.19 X_MSB_RESULT Register (Offset = 12h) [Reset = 0h]

X_MSB_RESULT is shown in Table 7-26.

Return to the Summary Table.

Table 7-26. X_MSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	X_CH_RESULT [15:8]	R	0h	X-channel data conversion results, MSB 8 bits.

7.5.1.20 X_LSB_RESULT Register (Offset = 13h) [Reset = 0h]

X_LSB_RESULT is shown in Table 7-27.

Return to the Summary Table.

Table 7-27. X_LSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	X_CH_RESULT [7:0]	R	0h	X-channel data conversion results, LSB 8 bits.

7.5.1.21 Y_MSB_RESULT Register (Offset = 14h) [Reset = 0h]

Y_MSB_RESULT is shown in Table 7-28.

Return to the Summary Table.

Table 7-28. Y_MSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Y_CH_RESULT [15:8]	R	0h	Y-channel data conversion results, MSB 8 bits.

7.5.1.22 Y_LSB_RESULT Register (Offset = 15h) [Reset = 0h]

Y_LSB_RESULT is shown in Table 7-29.

Return to the Summary Table.

Table 7-29. Y_LSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Y_CH_RESULT [7:0]	R	0h	Y-channel data conversion results, LSB 8 bits.

7.5.1.23 Z_MSB_RESULT Register (Offset = 16h) [Reset = 0h]

Z_MSB_RESULT is shown in Table 7-30.

Return to the Summary Table.

Table 7-30. Z_MSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Z_CH_RESULT [15:8]	R	0h	Z-channel data conversion results, MSB 8 bits.

7.5.1.24 Z_LSB_RESULT Register (Offset = 17h) [Reset = 0h]

Z_LSB_RESULT is shown in Table 7-31.

Return to the Summary Table.

Table 7-31. Z_LSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Z_CH_RESULT [7:0]	R	0h	Z-channel data conversion results, LSB 8 bits.

7.5.1.25 CONV_STATUS Register (Offset = 18h) [Reset = 0h]

CONV_STATUS is shown in Table 7-32.

Return to the Summary Table.

Table 7-32. CONV_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	SET_COUNT	R	0h	Rolling Count of Conversion Data Sets
4	POR	R/W1CP	0h	Device powered up, or experienced power-on-reset. Bit is clear when host writes back '1'. 0h = No POR 1h = POR occurred
3-2	RESERVED	R	0h	Reserved
1	DIAG_STATUS	R	0h	Detect any internal diagnostics fail which include VCC UV, internal memory CRC error, $\overline{INT}$ pin error and internal clock error. Ignore this bit status if VCC < 2.3V. 0h = No diag fail 1h = Diag fail detected
0	RESULT_STATUS	R	0h	Conversion data buffer is ready to be read. 0h = Conversion data not complete 1h = Conversion data complete

7.5.1.26 ANGLE_RESULT_MSB Register (Offset = 19h) [Reset = 0h]

ANGLE_RESULT_MSB is shown in Table 7-33.

Return to the Summary Table.

Table 7-33. ANGLE_RESULT_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ANGLE_RESULT_MSB	R	0h	Angle measurement result in degree. The data is displayed from 0 to 360 degree in 13 LSB bits after combining the ANGLE_RESULT_MSB and _LSB bits. The 4 LSB bits allocated for fraction of an angle in the format (xxxx/16).

7.5.1.27 ANGLE_RESULT_LSB Register (Offset = 1Ah) [Reset = 0h]

ANGLE_RESULT_LSB is shown in Table 7-34.

Return to the Summary Table.

Table 7-34. ANGLE_RESULT_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ANGLE_RESULT_LSB	R	0h	Angle measurement result in degree. The data is displayed from 0 to 360 degree in 13 LSB bits after combining the ANGLE_RESULT_MSB and _LSB bits. The 4 LSB bits allocated for fraction of an angle in the format (xxxx/16).

7.5.1.28 MAGNITUDE_RESULT Register (Offset = 1Bh) [Reset = 0h]

MAGNITUDE_RESULT is shown in Table 7-35.

Return to the Summary Table.

Table 7-35. MAGNITUDE_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAGNITUDE_RESULT	R	0h	Resultant vector magnitude (during angle measurement) result. This value should be constant during 360 degree measurements

7.5.1.29 DEVICE_STATUS Register (Offset = 1Ch) [Reset = 0h]

DEVICE_STATUS is shown in Table 7-36.

Return to the Summary Table.

Table 7-36. DEVICE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	INTB_RB	R	0h	Indicates the level that the device is reading back from $\overline{INT}$ pin. 0h = $\overline{INT}$ pin driven low 1h = $\overline{INT}$ pin status high
3	OSC_ER	R/W1CP	0h	Indicates if Oscillator error is detected. Bit is clear when host writes back '1'. 0h = No Oscillator error detected 1h = Oscillator error detected
2	INT_ER	R/W1CP	0h	Indicates if $\overline{INT}$ pin error is detected. Bit is clear when host writes back '1'. 0h = No $\overline{INT}$ error detected 1h = $\overline{INT}$ error detected
1	OTP_CRC_ER	R/W1CP	0h	Indicates if OTP CRC error is detected. Bit is clear when host writes back '1'. 0h = No OTP CRC error detected 1h = OTP CRC error detected
0	VCC_UV_ER	R/W1CP	0h	Indicates if VCC undervoltage was detected. Bit is clear when host writes back '1'. Ignore this bit status if VCC < 2.3V. 0h = No VCC UV detected 1h = VCC UV detected

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Select the Sensitivity Option

Select the highest TMAG5273 sensitivity option that can measure the required range of magnetic flux density so that the ADC output range is maximized.

Larger-sized magnets and farther sensing distances can generally enable better positional accuracy than very small magnets at close distances, because magnetic flux density increases exponentially with the proximity to a magnet. TI created an online tool to help with simple magnet calculations under the DRV5055 product folder on ti.com.

8.1.2 Temperature Compensation for Magnets

The TMAG5273 temperature compensation is designed to directly compensate the average temperature drift of several magnets as specified in the MAG_TEMPCO register bits. The residual induction (B_r) of a magnet typically reduces by 0.12%/°C for NdFeB, and 0.20%/°C for ferrite magnets as the temperature increases. Set the MAG_TEMPCO bit to default 00b if the device temperature compensation is not needed.

8.1.3 Sensor Conversion

Multiple conversion schemes can be adopted based off the MAG_CH_EN and CONV_AVG register bits setting.

8.1.3.1 Continuous Conversion

The TMAG5273 can be set in continuous conversion mode when OPERATING_MODE is set to 10b. Figure 8-1 shows few examples of continuous conversion. The input magnetic field is processed in two steps. In the first step the device spins the hall sensor elements, and integrates the sampled data. In the second step the ADC block coverts the analog signal into digital bits and stores in the corresponding result register. While the ADC starts processing the first magnetic sample, the spin block can start processing another magnetic sample. In this mode the temperature data is taken at the beginning of each new conversion. This temperature data is used to compensate for the thermal drift.

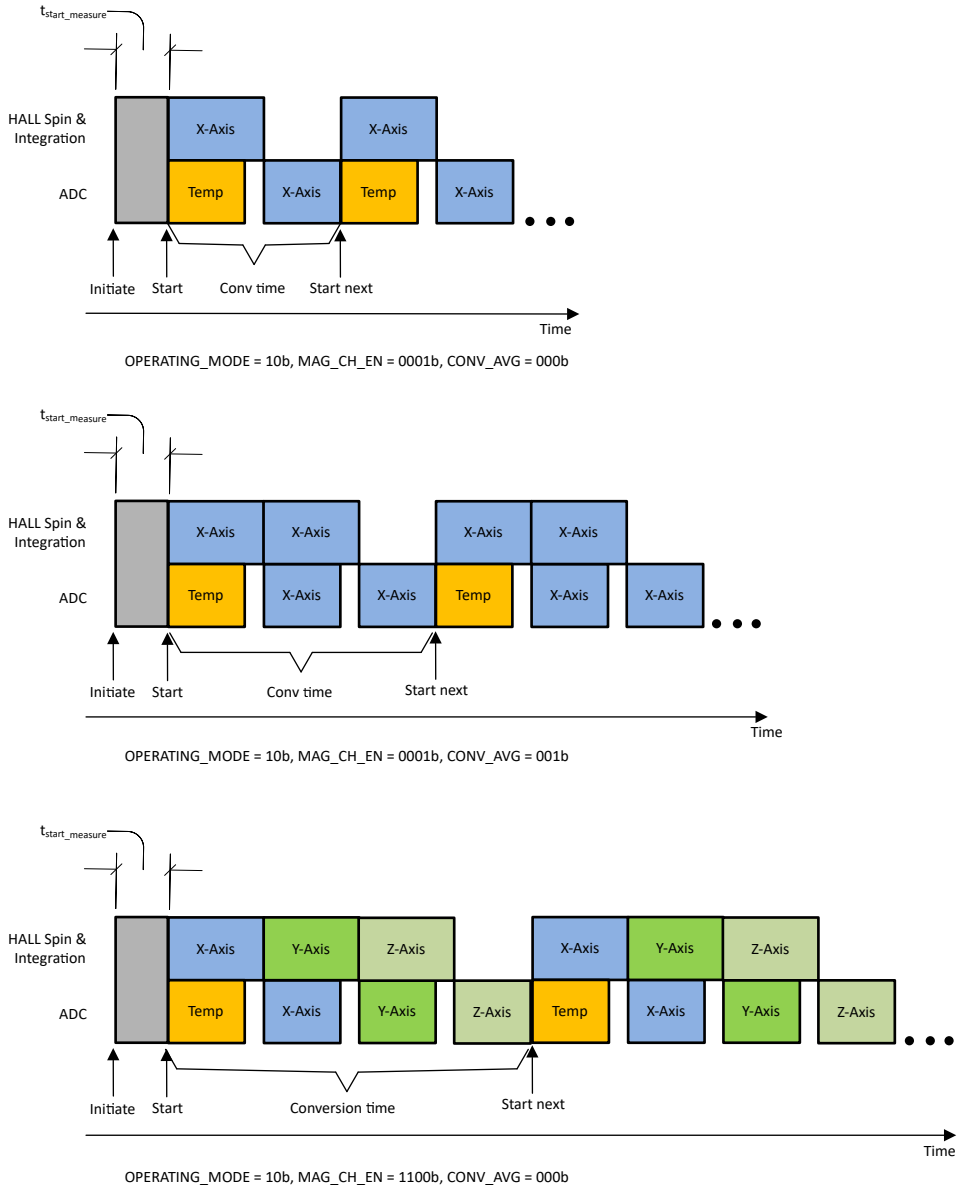

Figure 8-1. Continuous Conversion Examples

8.1.3.2 Trigger Conversion

The TMAG5273 supports trigger conversion with OPERATING_MODE set to 00b. The trigger event can be initiated through I^2C command or $\overline{INT}$ signal. Figure 8-2 shows an example of trigger conversion with temperature, X, Y, and Z sensors activated.

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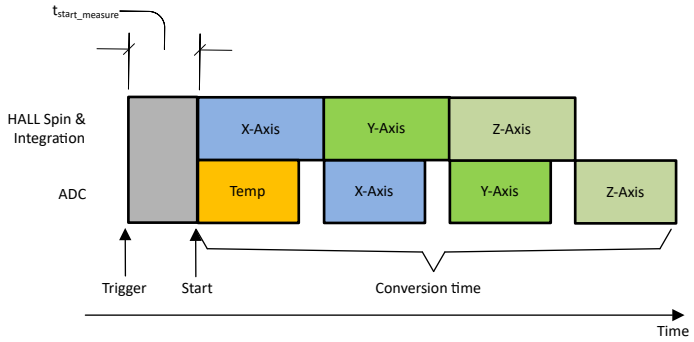

Figure 8-2. Trigger Conversion for Temperature, X, Y, & Z Sensors

8.1.3.3 Pseudo-Simultaneous Sampling

In absolute angle measurement, application sensor data from multiple axes are required to calculate an accurate angle. The magnetic field data collected at different times through the same signal chain introduces error in angle calculation. The TMAG5273 offers pseudo-simultaneous sampling data collection modes to eliminate this error. Figure 8-3 shows an example where MAG_CH_EN is set at 1011b to collect XZX data. The time stamps for X and Z sensor data are the same as shown in Equation 17.

$$t_Z = \frac{t_{X1} + t_{X2}}{2} \tag{17}$$

where

- t_{X1}, t_Z, t_{X2} are time stamps for X, Z, X sensor data completion as defined in Figure 8-3.

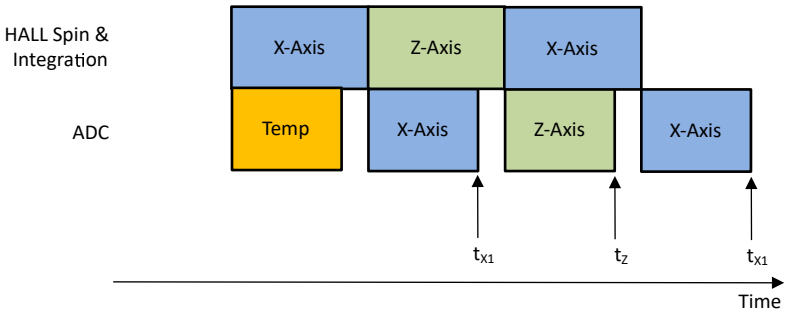

Figure 8-3. XZX Magnetic Field Conversion

The vertical X, Y sensors of the TMAG5273 exhibit more noise than the horizontal Z sensor. The pseudo-simultaneous sampling can be used to equalize the noise floor when two set of vertical sensor data are collected against one set of horizontal sensor data, as in examples of XZX or YZY modes.

8.1.4 Magnetic Limit Check

The TMAG5273 enables magnetic limit checks for single or multiple axes at the same time. Figure 8-4 to Figure 8-7 show examples of magnetic limit cross detection events while the field going above, below, exiting a magnetic band, and entering a magnetic band. The device will keep generating interrupt with each new conversion if the magnetic fields remain in the shaded regions in the figures. The MAG_THR_DIR and THR_HYST register bits help select different limit cross modes.

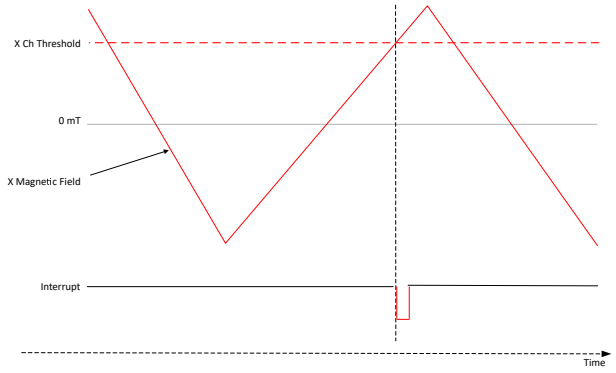

Figure 8-4. Magnetic Upper Limit Cross Check With MAG_THR_DIR =0b, THR_HYST = 000b

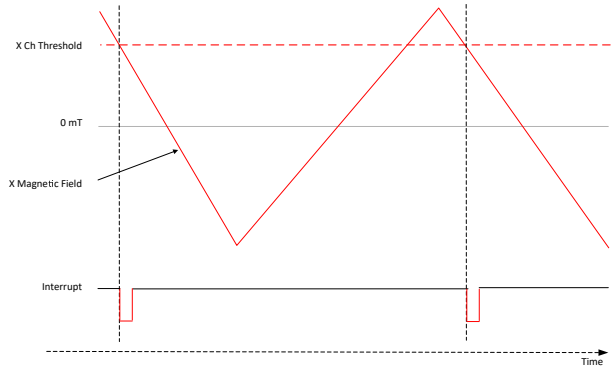

Figure 8-5. Magnetic Lower Limit Cross Check With MAG_THR_DIR =1b, THR_HYST = 000b

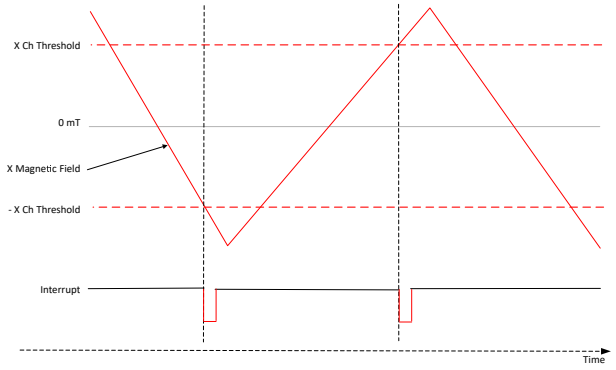

Figure 8-6. Magnetic Field Going Out of Band Check With MAG_THR_DIR =0b, THR_HYST = 001b

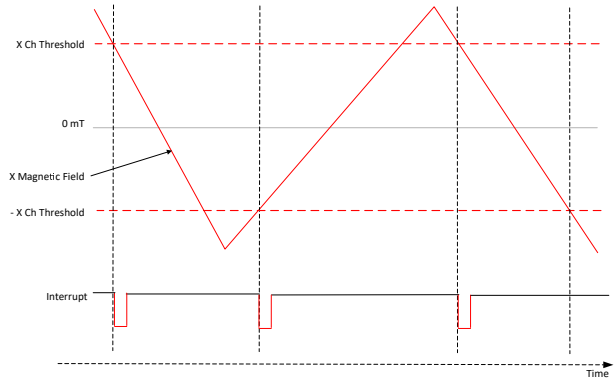

Figure 8-7. Magnetic Field Entering a Band Check With MAG_THR_DIR =1b, THR_HYST = 001b

8.2 Typical Application

Magnetic angle sensors are very popular due to contactless and reliable measurements, especially in applications requiring long-term measurements in rugged environments. The TMAG5273 offers an on-chip angle calculator providing angular measurement based off any two of the magnetic axes. The two axes of interest can be selected in the ANGLE_EN register bits. The device offers angle output in complete 360 degree scale. Take several error sources into account for angle calculation, including sensitivity error, offset error, linearity error, noise, mechanical vibration, temperature drift, and so forth.

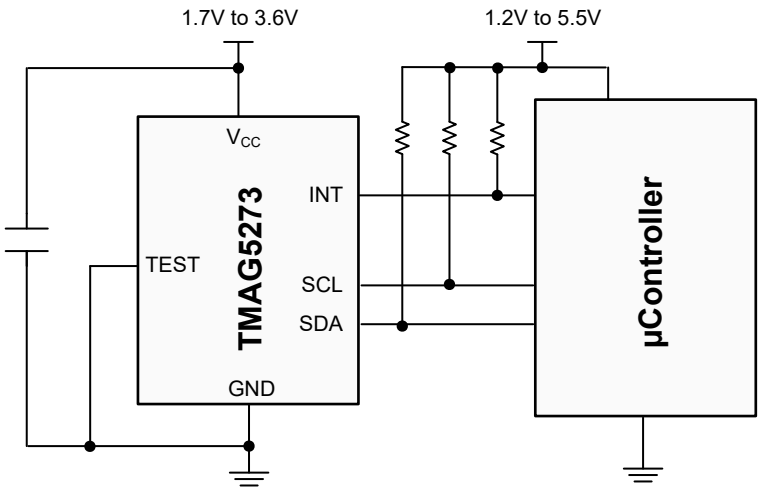

Figure 8-8. TMAG5273 Application Diagram

ADVANCE INFORMATION

8.2.1 Design Requirements

Use the parameters listed in Table 8-1 for this design example

Table 8-1. Design Parameters

DESIGN PARAMETERS	ON-AXIS MEASUREMENT	OFF-AXIS MEASUREMENT
Device	TMAG5273-A1	TMAG5273-A1
VCC	3.3 V	3.3 V
Magnet	Cylinder: 4.7625-mm diameter, 12.7-mm thick, neodymium N52, Br = 1480	Cylinder: 4.7625-mm diameter, 12.7-mm thick, neodymium N52, Br = 1480
Magnetic Range Selection	Select the same range for both axes based off the highest possible magnetic field seen by the sensor	Select the same range for both axes based off the highest possible magnetic field seen by the sensor
RPM	<600	<600
Desired Accuracy	<2° for 360° rotation	<2° for 360° rotation

8.2.2 Detailed Design Procedure

For accurate angle measurement, the two axes amplitudes must be normalized by selecting the proper gain adjustment value in the MAG_GAIN_CONFIG register. The gain adjustment value is a fractional decimal number between 0 and 1. The following steps must be followed to calculate this fractional value:

- Set the device at 32x average mode and rotate the shaft full 360 degree.
- Record the two axes sensor ADC codes for the full 360 degree rotation.
- Measure the maximum peak-peak ADC code delta for each axis, Ax and Ay as shown in Figure 8-10 or Figure 8-11.
- If $A_X > A_Y$, set the MAG_GAIN_CH register bit to 0h. Calculate the gain adjustment value for X axis: $G_X = \frac{A_Y}{A_X}$
- If $A_X < A_Y$, set the MAG_GAIN_CH register bit to 1h. Calculate the gain adjustment value for Y axis: $G_Y = \frac{1}{G_X}$
- The target binary gain setting at the GAIN_VALUE register bits are calculated from the equation, G_X or G_Y = $GAIN\_VALUE_{decimal}$/ 1024.

Example 1: If $A_X = A_Y$ = 60,000, the GAIN_VALUE register bits are set at default 0h.

Example 2: If A_X= 60,000, A_Y = 45,000, the G_X = 45,000/60,000 =0.75.

Example 3: If A_X= 45,000, A_Y = 60,000, the G_X = (60,000/45,000) =1.33. Since G_X >1, the gain adjustment needs to be applied to Y axis with $G_Y = 1/G_X$

8.2.2.1 Gain Adjustment for Angle Measurement

Common measurement topology include angular position measurements in on-axis or off-axis angular measurements shown in Figure 8-9. Select the on-axis measurement topology whenever possible as this offers the best optimization of magnetic field and the device measurement ranges. The TMAG5273 offers on-chip gain adjustment option to account for mechanical position misalignments.

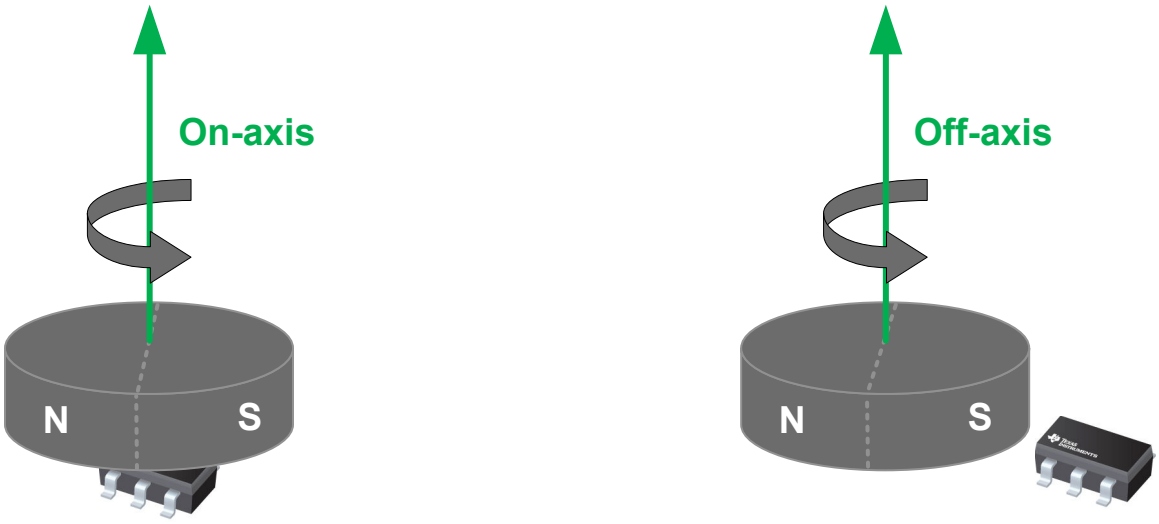

Figure 8-9. On-Axis vs. Off-Axis Angle Measurements

8.2.3 Application Curves

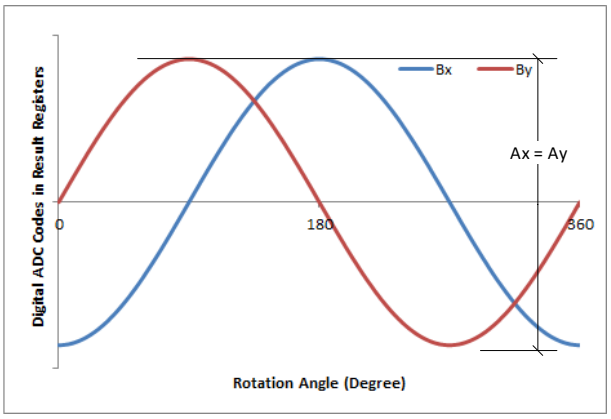

Figure 8-10. X and Y Sensor Data for Full 360 Degree Rotation for On-Axis Measurement

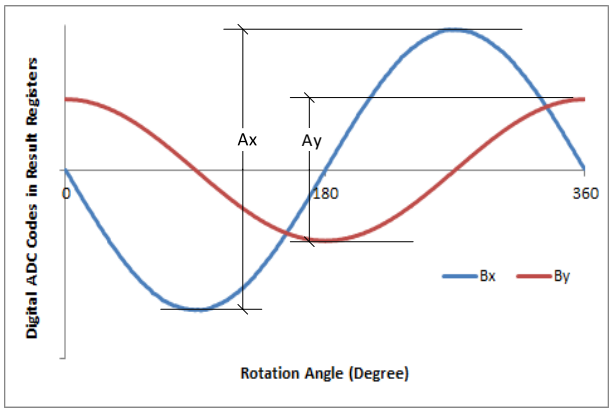

Figure 8-11. X and Y Sensor Data for Full 360 Degree Rotation for Off-Axis Measurement

8.3 What to Do and What Not to Do

The TMAG5273 updates the result registers at the end of a conversion. I^2C read of the result register needs to be synchronized with the conversion update time to avoid reading a result data while the result register is being updated. For applications with tight timing budget use the $\overline{INT}$ signal to notify the primary when a conversion is complete.

9 Power Supply Recommendations

A decoupling capacitor close to the device must be used to provide local energy with minimal inductance. TI recommends using a ceramic capacitor with a value of at least 0.01 µF. Connect the TEST pin to ground.

ADVANCE INFORMATION

10 Layout

10.1 Layout Guidelines

Magnetic fields pass through most nonferromagnetic materials with no significant disturbance. Embedding Hall effect sensors within plastic or aluminum enclosures and sensing magnets on the outside is common practice. Magnetic fields also easily pass through most printed-circuit boards (PCBs), which makes placing the magnet on the opposite side of the PCB possible.

10.2 Layout Example

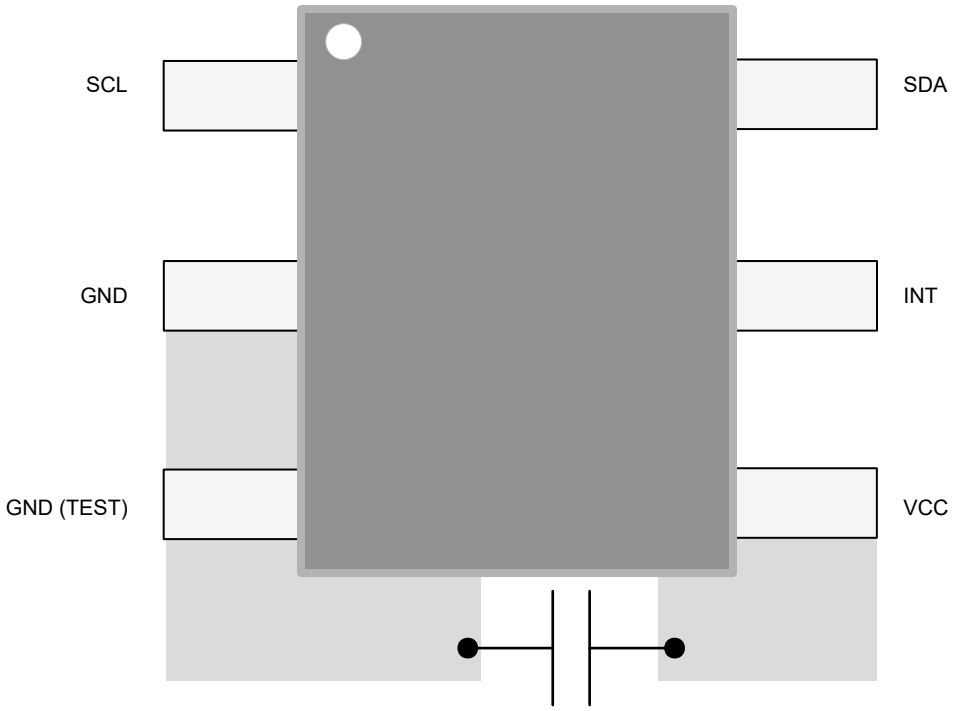

Figure 10-1. Layout Example With TMAG5273

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *HALL-ADAPTER-EVM User's Guide* (SLYU043)
- Texas Instruments, *TMAG5273 Evaluation Manual user's guide* (SLYU058)
- Texas Instruments, *Angle Measurement With Multi-Axis Linear Hall-Effect Sensors* application report (SBAA463)
- Texas Instruments, *Absolute Angle Measurements for Rotational Motion Using Hall-Effect Sensors* application brief (SBAA503)
- Texas Instruments, *Limit Detection for Tamper and End-of-Travel Detection Using Hall-Effect Sensors* application brief (SBOA514)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

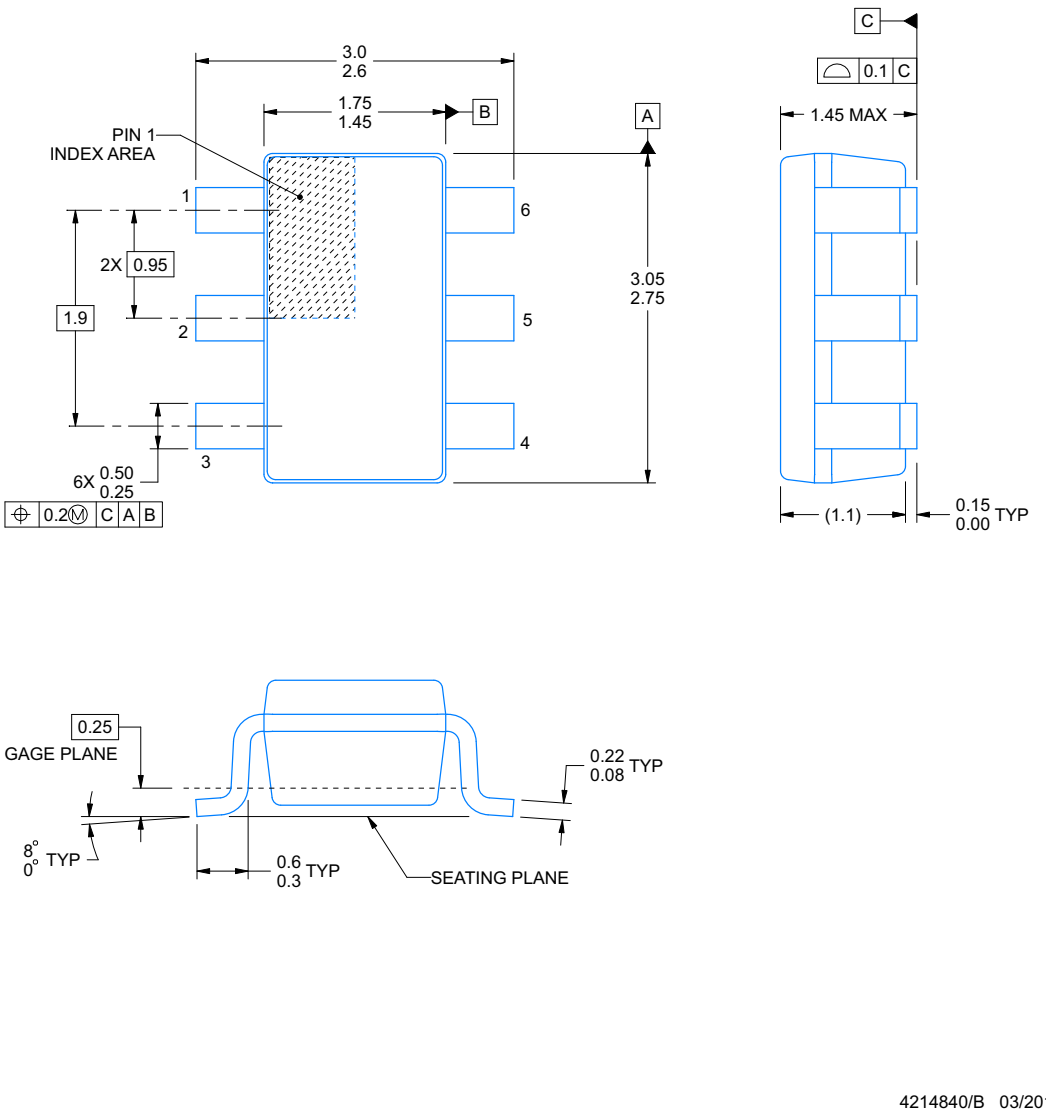
ADVANCE INFORMATION

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.

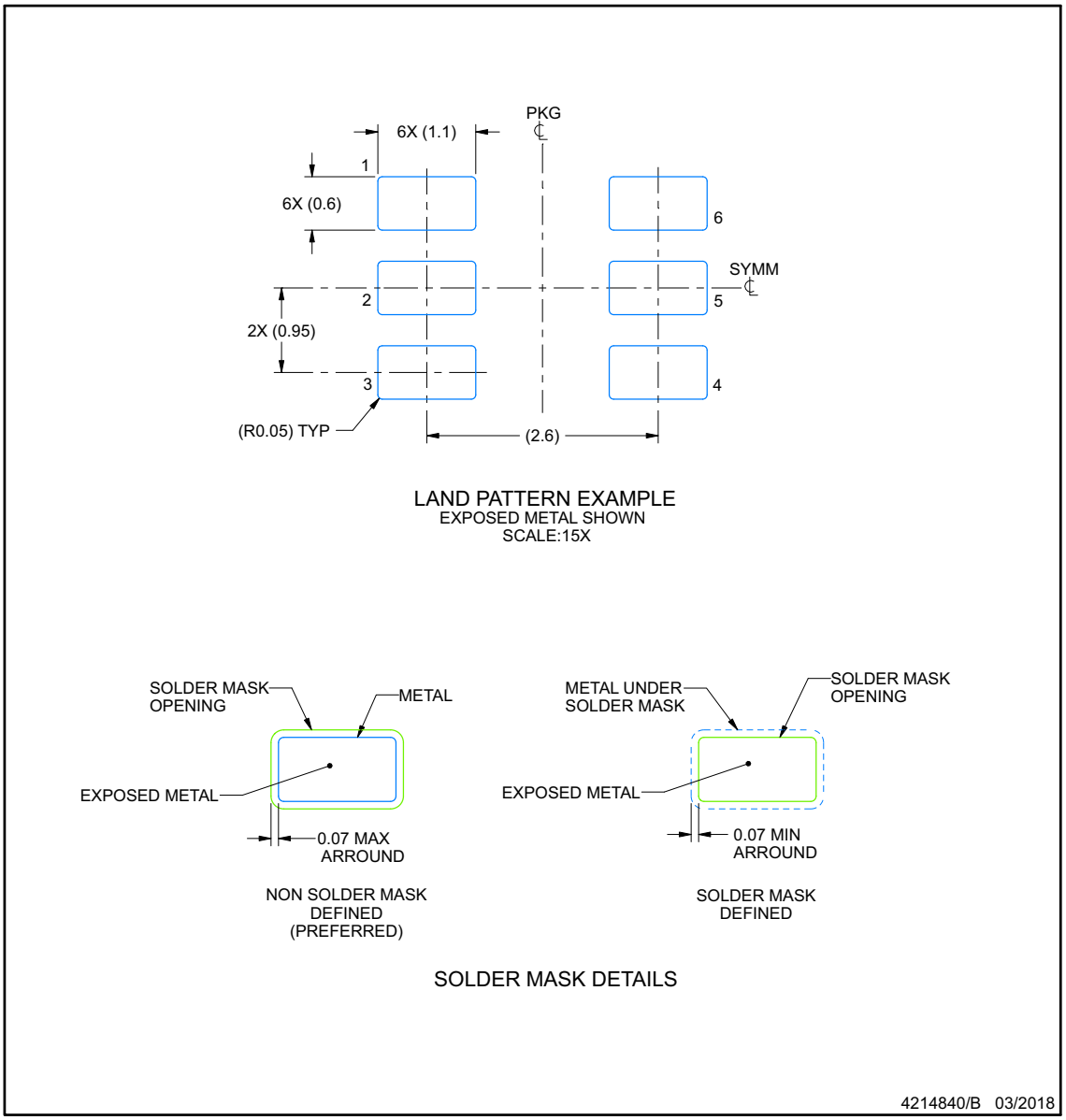
www.ti.com

Figure 12-1. DBV Package Outline

EXAMPLE BOARD LAYOUT

DBV0006A — **SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



NOTES: (continued)

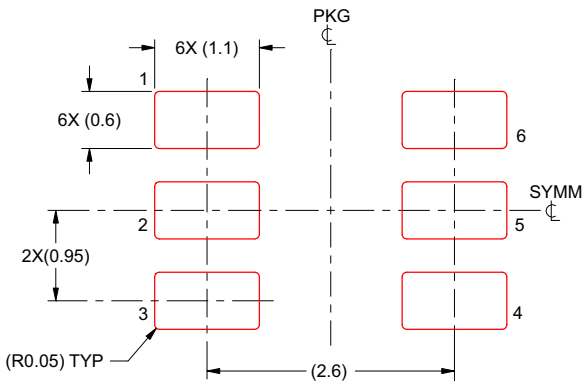
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

Figure 12-2. DBV Package Board Layout

EXAMPLE STENCIL DESIGN

DBV0006A — **SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

Figure 12-3. DBV Package Stencil Outline

12.1 Package Option Addendum

Packaging Information

Orderable	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
TMAG5273A1Q DBVR	ACTIVE	SOT-23	DBV	6	Call TI	Non-RoHS & Non-Green	Call TI	Call TI	Call TI	Call TI
TMAG5273A1Q DBVT	ACTIVE	SOT-23	DBV	6	Call TI	Non-RoHS & Non-Green	Call TI	Call TI	Call TI	Call TI
TMAG5273A2Q DBVR	ACTIVE	SOT-23	DBV	6	Call TI	Non-RoHS & Non-Green	Call TI	Call TI	Call TI	Call TI
TMAG5273A2Q DBVT	ACTIVE	SOT-23	DBV	6	Call TI	Non-RoHS & Non-Green	Call TI	Call TI	Call TI	Call TI
TMAG5273A3Q DBVR	ACTIVE	SOT-23	DBV	6	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
TMAG5273A3Q DBVT	ACTIVE	SOT-23	DBV	6	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
TMAG5273A4Q DBVR	ACTIVE	SOT-23	DBV	6	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
TMAG5273A4Q DBVT	ACTIVE	SOT-23	DBV	6	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
TMAG5273B1Q DBVR	ACTIVE	SOT-23	DBV	6	Call TI	Non-RoHS & Non-Green	Call TI	Call TI	Call TI	Call TI
TMAG5273B1Q DBVT	ACTIVE	SOT-23	DBV	6	Call TI	Non-RoHS & Non-Green	Call TI	Call TI	Call TI	Call TI
TMAG5273B2Q DBVR	ACTIVE	SOT-23	DBV	6	Call TI	Non-RoHS & Non-Green	Call TI	Call TI	Call TI	Call TI
TMAG5273B2Q DBVT	ACTIVE	SOT-23	DBV	6	Call TI	Non-RoHS & Non-Green	Call TI	Call TI	Call TI	Call TI
TMAG5273B3Q DBVR	ACTIVE	SOT-23	DBV	6	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
TMAG5273B3Q DBVT	ACTIVE	SOT-23	DBV	6	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
TMAG5273B4Q DBVR	ACTIVE	SOT-23	DBV	6	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
TMAG5273B4Q DBVT	ACTIVE	SOT-23	DBV	6	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
TMAG5273C1 QDBVR	ACTIVE	SOT-23	DBV	6	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI

ADVANCE INFORMATION

Orderable	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
TMAG5273C1 QDBVT	ACTIVE	SOT-23	DBV	6	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
TMAG5273C2 QDBVR	ACTIVE	SOT-23	DBV	6	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
TMAG5273C2 QDBVT	ACTIVE	SOT-23	DBV	6	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
TMAG5273D1 QDBVR	ACTIVE	SOT-23	DBV	6	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
TMAG5273D1 QDBVT	ACTIVE	SOT-23	DBV	6	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
TMAG5273D2 QDBVR	ACTIVE	SOT-23	DBV	6	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
TMAG5273D2 QDBVT	ACTIVE	SOT-23	DBV	6	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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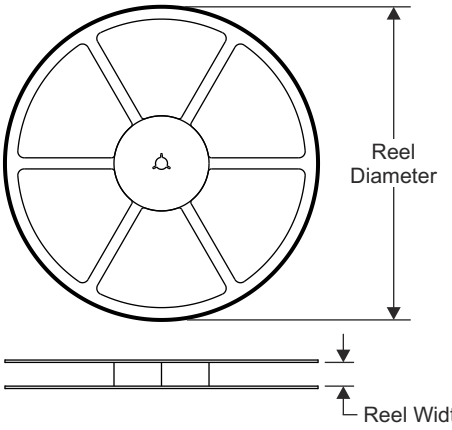
ADVANCE INFORMATION

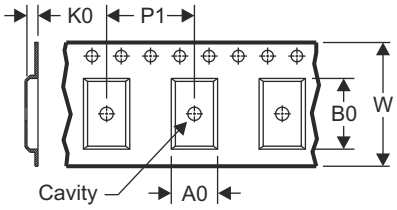
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

12.2 Tape and Reel Information

REEL DIMENSIONS

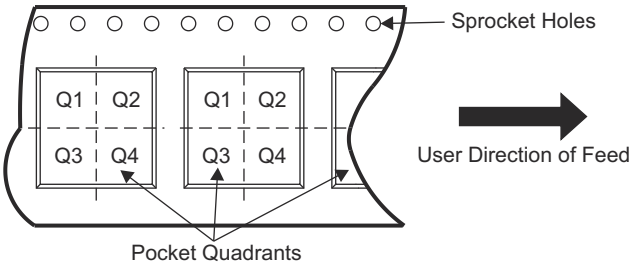


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

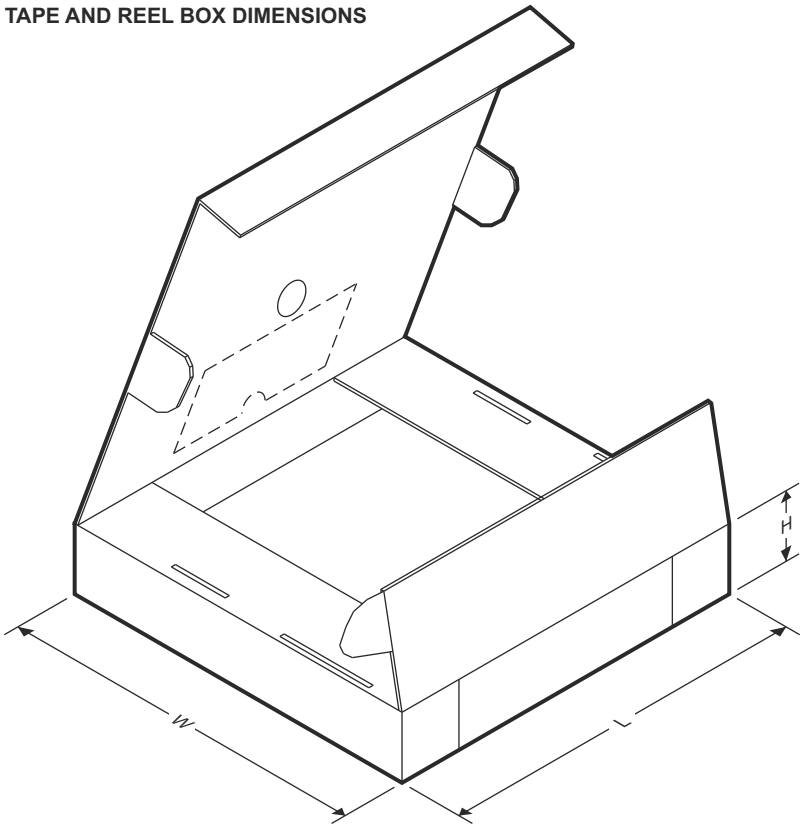
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMAG5273A1QDBVR	SOT-23	DBV	6	3000								
TMAG5273A1QDBVT	SOT-23	DBV	6	250								
TMAG5273A2QDBVR	SOT-23	DBV	6	3000								
TMAG5273A2QDBVT	SOT-23	DBV	6	250								
TMAG5273A3QDBVR	SOT-23	DBV	6	3000								
TMAG5273A3QDBVT	SOT-23	DBV	6	250								
TMAG5273A4QDBVR	SOT-23	DBV	6	3000								
TMAG5273A4QDBVT	SOT-23	DBV	6	250								
TMAG5273B1QDBVR	SOT-23	DBV	6	3000								
TMAG5273B1QDBVT	SOT-23	DBV	6	250								
TMAG5273B2QDBVR	SOT-23	DBV	6	3000								
TMAG5273B2QDBVT	SOT-23	DBV	6	250								
TMAG5273B3QDBVR	SOT-23	DBV	6	3000								
TMAG5273B3QDBVT	SOT-23	DBV	6	250								
TMAG5273B4QDBVR	SOT-23	DBV	6	3000								
TMAG5273B4QDBVT	SOT-23	DBV	6	250								
TMAG5273C1QDBVR	SOT-23	DBV	6	3000								
TMAG5273C1QDBVT	SOT-23	DBV	6	250								
TMAG5273C2QDBVR	SOT-23	DBV	6	3000								
TMAG5273C2QDBVT	SOT-23	DBV	6	250								
TMAG5273D1QDBVR	SOT-23	DBV	6	3000								
TMAG5273D1QDBVT	SOT-23	DBV	6	250								
TMAG5273D2QDBVR	SOT-23	DBV	6	3000								
TMAG5273D2QDBVT	SOT-23	DBV	6	250								

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMAG5273A1QDBVR	SOT-23	DBV	6	3000	Call TI	Call TI	Call TI
TMAG5273A1QDBVT	SOT-23	DBV	6	250	Call TI	Call TI	Call TI
TMAG5273A2QDBVR	SOT-23	DBV	6	3000	Call TI	Call TI	Call TI
TMAG5273A2QDBVT	SOT-23	DBV	6	250	Call TI	Call TI	Call TI
TMAG5273A3QDBVR	SOT-23	DBV	6	3000	Call TI	Call TI	Call TI
TMAG5273A3QDBVT	SOT-23	DBV	6	250	Call TI	Call TI	Call TI
TMAG5273A4QDBVR	SOT-23	DBV	6	3000	Call TI	Call TI	Call TI
TMAG5273A4QDBVT	SOT-23	DBV	6	250	Call TI	Call TI	Call TI
TMAG5273B1QDBVR	SOT-23	DBV	6	3000	Call TI	Call TI	Call TI
TMAG5273B1QDBVT	SOT-23	DBV	6	250	Call TI	Call TI	Call TI
TMAG5273B2QDBVR	SOT-23	DBV	6	3000	Call TI	Call TI	Call TI
TMAG5273B2QDBVT	SOT-23	DBV	6	250	Call TI	Call TI	Call TI
TMAG5273B3QDBVR	SOT-23	DBV	6	3000	Call TI	Call TI	Call TI
TMAG5273B3QDBVT	SOT-23	DBV	6	250	Call TI	Call TI	Call TI
TMAG5273B4QDBVR	SOT-23	DBV	6	3000	Call TI	Call TI	Call TI
TMAG5273B4QDBVT	SOT-23	DBV	6	250	Call TI	Call TI	Call TI
TMAG5273C1QDBVR	SOT-23	DBV	6	3000	Call TI	Call TI	Call TI
TMAG5273C1QDBVT	SOT-23	DBV	6	250	Call TI	Call TI	Call TI
TMAG5273C2QDBVR	SOT-23	DBV	6	3000	Call TI	Call TI	Call TI
TMAG5273C2QDBVT	SOT-23	DBV	6	250	Call TI	Call TI	Call TI
TMAG5273D1QDBVR	SOT-23	DBV	6	3000	Call TI	Call TI	Call TI
TMAG5273D1QDBVT	SOT-23	DBV	6	250	Call TI	Call TI	Call TI
TMAG5273D2QDBVR	SOT-23	DBV	6	3000	Call TI	Call TI	Call TI

ADVANCE INFORMATION

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMAG5273D2QDBVT	SOT-23	DBV	6	250	Call TI	Call TI	Call TI

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMAG5273A2QDBVR	ACTIVE	SOT-23	DBV	6	3000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

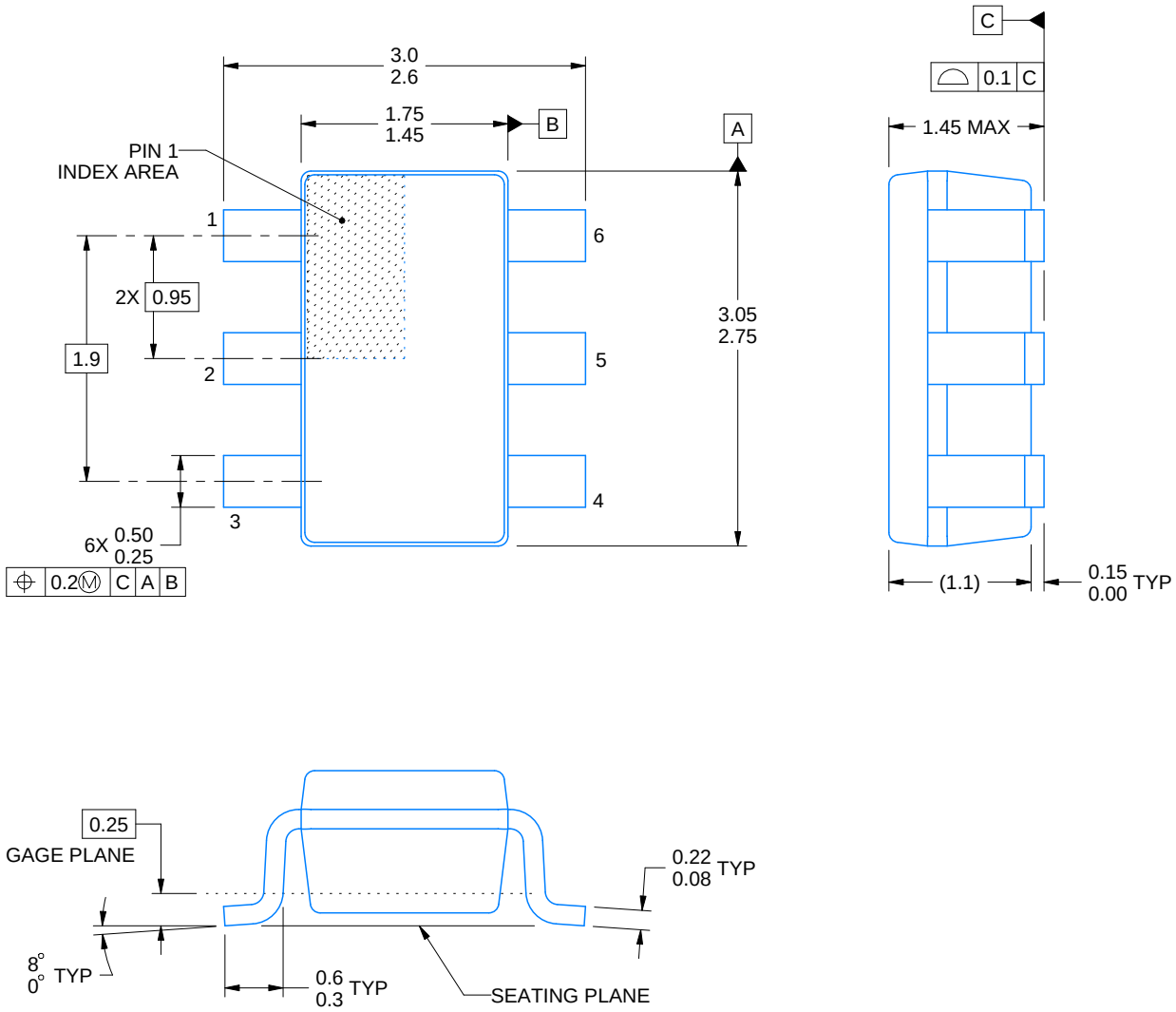
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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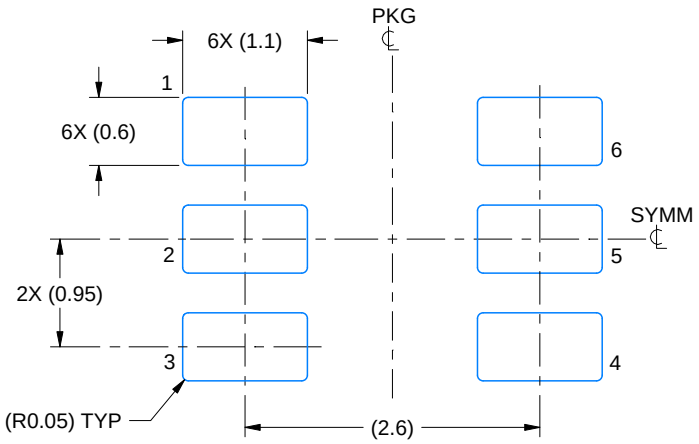
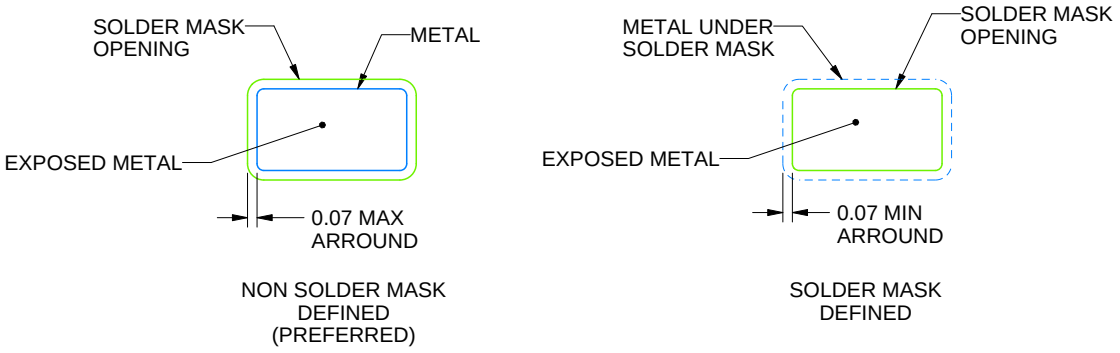
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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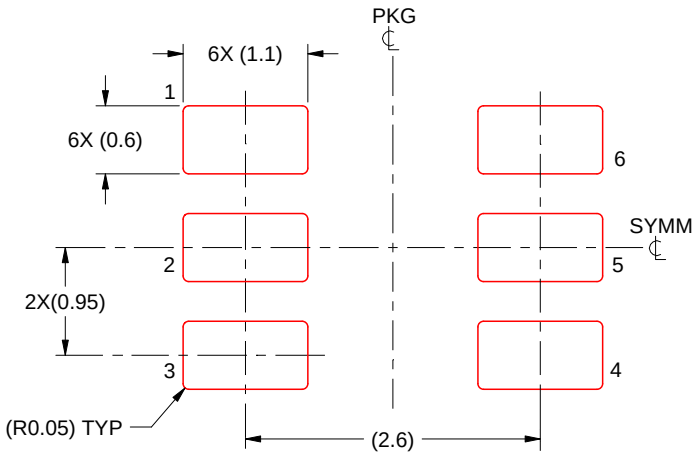
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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