Future of COMPASS Trigger

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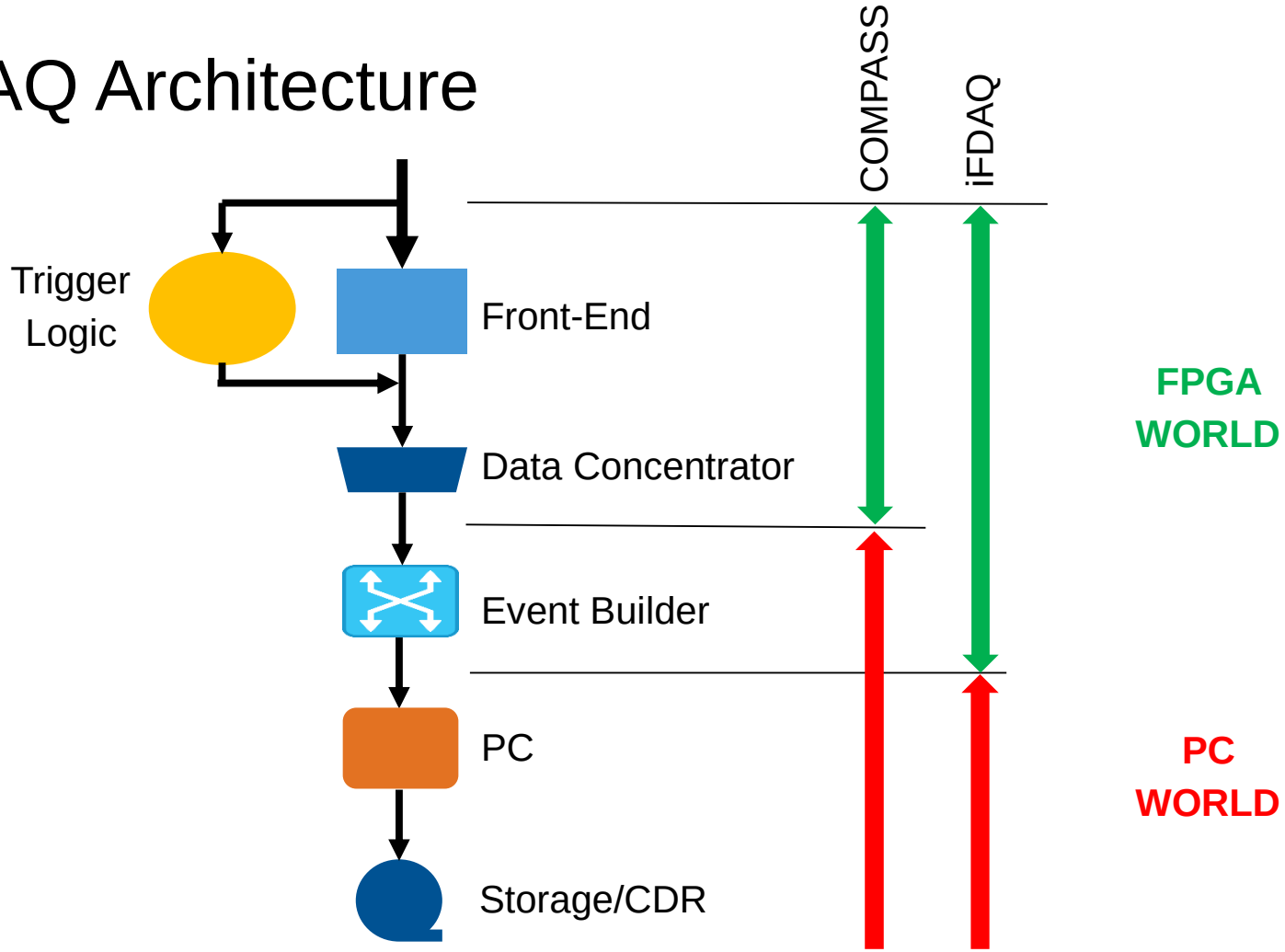
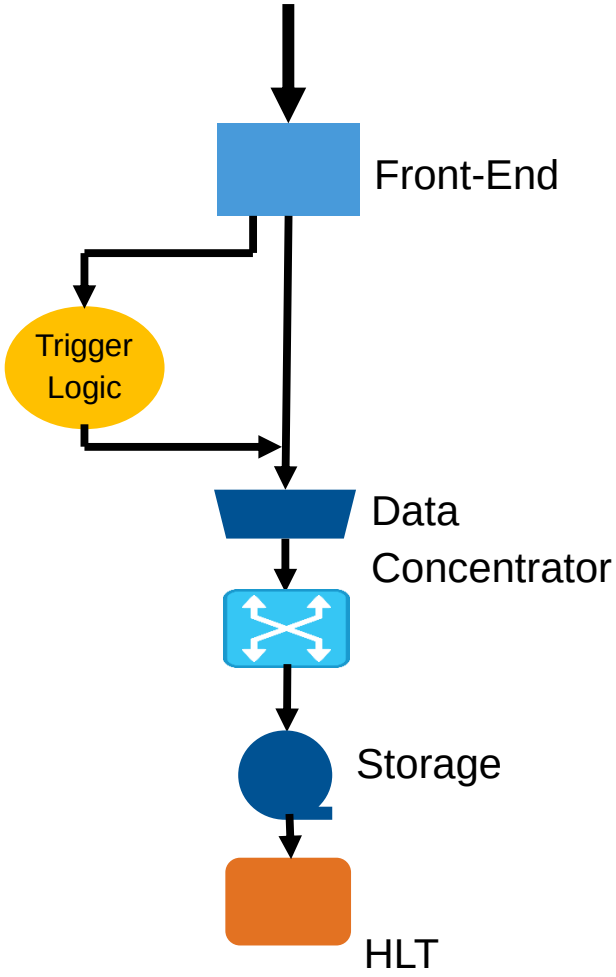
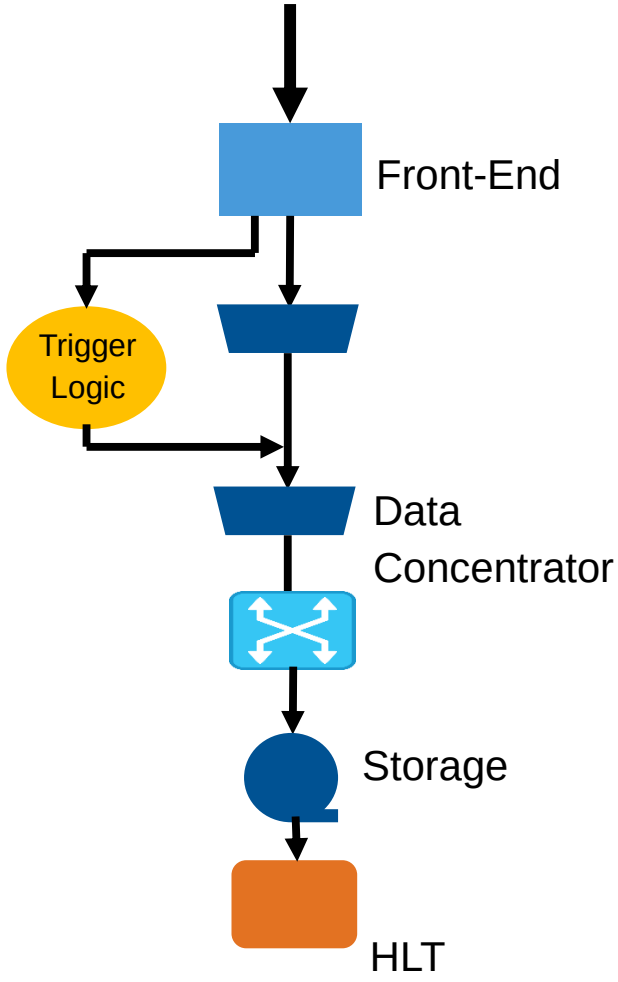
DAQ Architecture



Possible DAQ Architecture





New Developments

DAQ Upgrade

IPBUS interface developed for CMS

- UDP based protocol
- Direct Ethernet connection to FPGA to access internal registers , memories
- Requires little FPGA resources

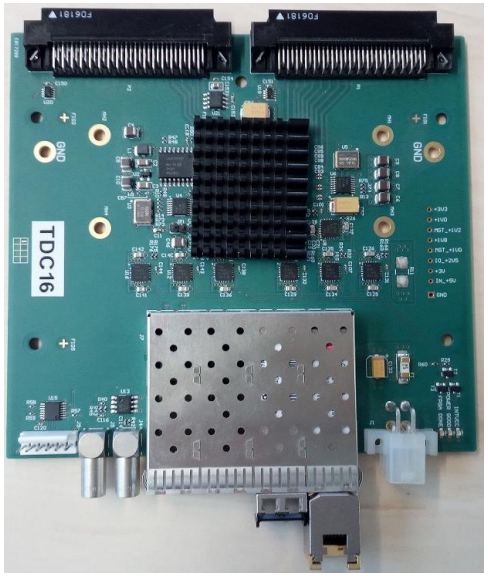
UCF (Unified Communication Framework)

- Protocol for serial links
- Universal protocol for all types of communications between FPGAs
- Single link for trigger, slow control(IPBUS) and data
- Supports point-to-point and start like topology

FPGA TDC - iFTDC

New Kintex Ultrascale FPGA module for DAQ and Trigger Processor

iFTDC



Features

- ARTIX7 FPGA
- 64 TDC channels
- Bin size : 1 ns, 0.6 ns, 0.3 ns (32 channels)
- Time resolution : 300ps, 200 ps, 100 ps
- PCB exists for MWPC, DC00-DC04
- TDC price ~5 Euro/channel
- It's planned to use the module for CEDAR in 2018
- **Unified interfaces**
  - UCF to TDC MUX 2.5 Gbps , triggered data
  - UCF to Trigger processor , trigger less data

Requirements for new FEE :

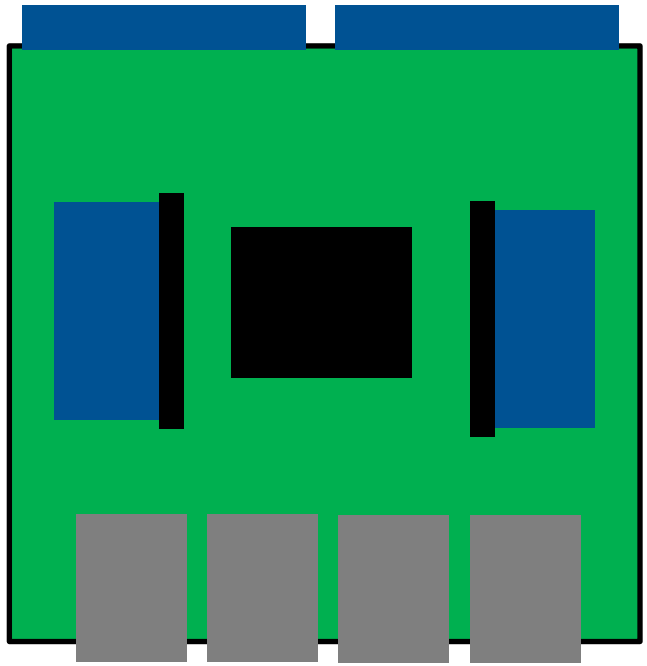
- two high speed serial links
- UCF protocol for integration to DAQ
- TUM will provide UCF ip cores

Development of Kintex UltraScale DAQ Module

Technical parameters :

- XCKU095-A1156
  - 1.2 M logic cells
  - 60 Mbit Block RAM
  - 64 x 16Gb/s
- **2 x 16 GB DDR4 SODIMM, combined data throughput 10 GB/s**
- AMC connector Interfaces
  - TCS
  - Ethernet(IPBUS)
  - 15 x 16Gb/s
- Front panel interfaces
  - 48 x 16Gb/s

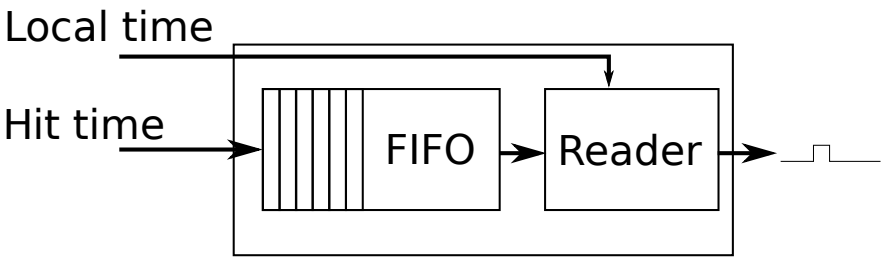
Applications : Data Concentrator, Event Builder, Trigger



FPGA-based Digital Trigger Logic

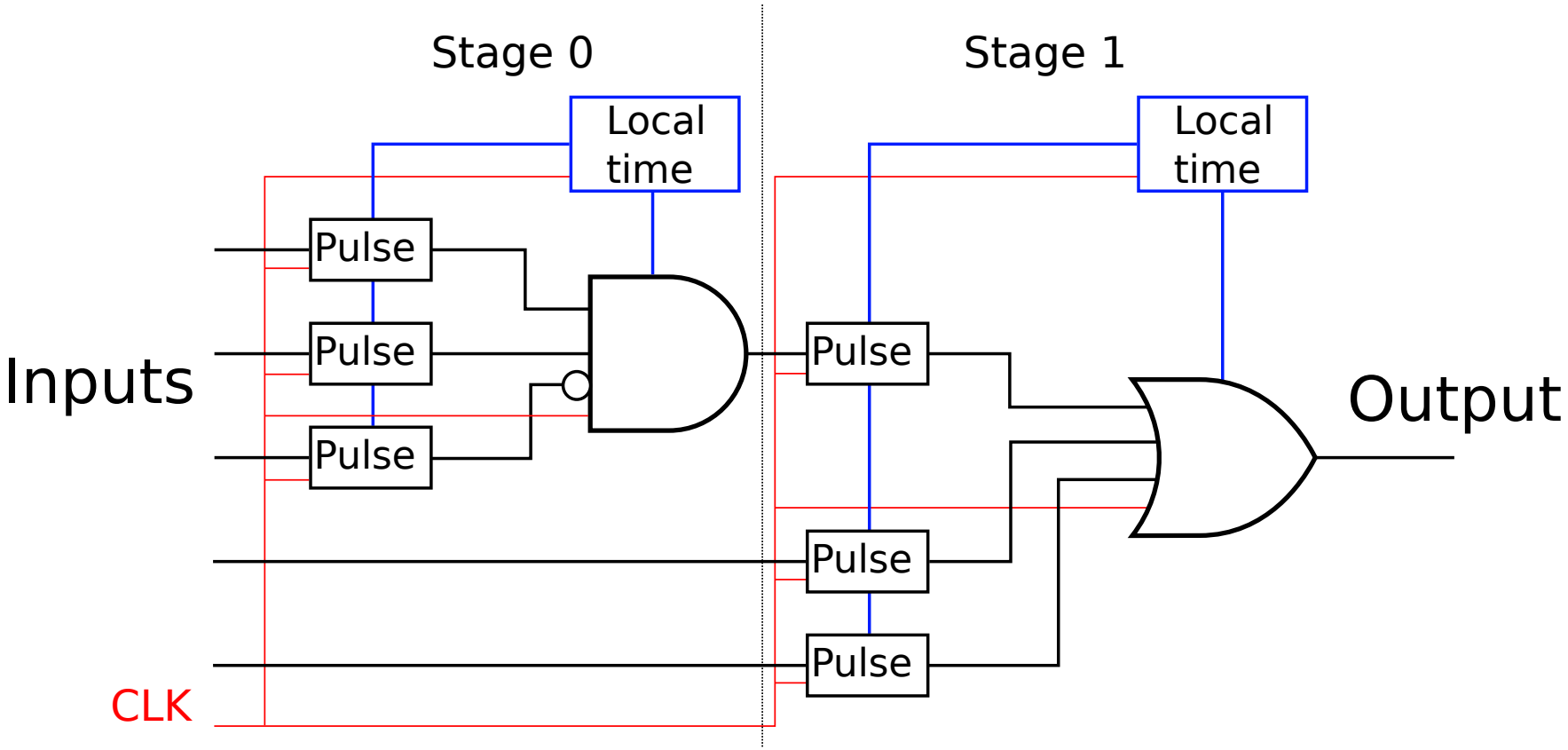
- Was developed in 2010-2011 as a student project for evaluation of the FPGA-based trigger architecture with integrated TDC
  - Project stopped at the simulation stage
- Cores to process hits in pipeline
  - Local time processing
  - Pulse processing
  - Coincidence/Anti-coincidence (logic AND), aggregation (logic OR)
- Configuration of the trigger logic layout out of the available cores independent of implementation
- Software for automatic generation of VHDL code from the configuration file
- Requirement:
  - all hits are assigned a timestamp using the global time
  - Hit time format:
    - Coarse time: timestamp from the global time
    - Fine time: sub-system clock resolution from the measurement

Pulse Processing



- Re-synchronization of the channels
- Buffer hits in FIFO
- Generate a pulse at the hit time
  $t_{hit} = t_{local} + const$
  - constant for aligning different channels
- Requirements:
  - Hits received ordered in time
  - Deterministic maximal hit latency

Trigger Logic Layout



Next Steps

Rebuild current trigger design (matrix and nim logic) in timestamp logic

- Basic Requiments:
  - T_0 correction of signals
  - meantimer-logic
  - NxM matrix coincidence of signals
  - veto logic
  - monitoring of signal on different stages
  - time resolution:
    delay stages resolution 250 ps
  - ... ?

With already installed lvds-splitter parallel operation and development with current trigger system possible.

Next: Determination of platform for first tests.

Proton Radius Measurement

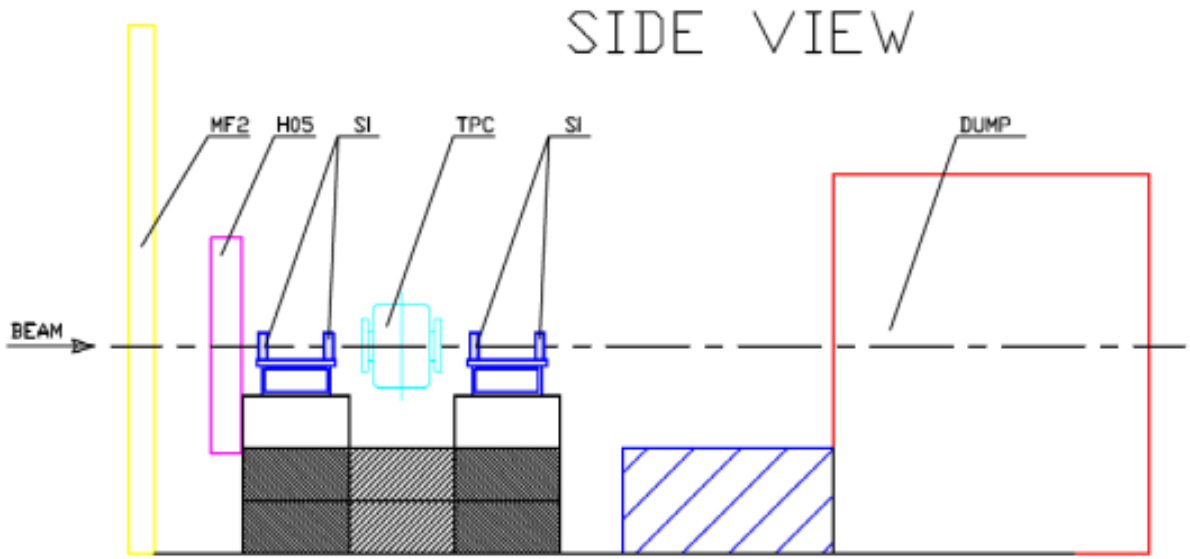
- 100 GeV muons on H_2-Target with 4-20bar
- Interesting region: $0.001 < Q^2/\frac{GeV^2}{c^2} < 0.02$
- TPC for recoil proton tracks
- Cylindric array of scifi arround target
- Muon kinematics through compass Spectrometer

Triggering only on proton recoil leads to Q^2 depended efficiencies

new Beam Trigger

- Veto tracks <5 μrad
  $\rightarrow$ suppress muons with only multiple small scattering
  (99% of incoming rate.)
- from 100μrad on efficient selection in the target.

PRM Testsetup 2018



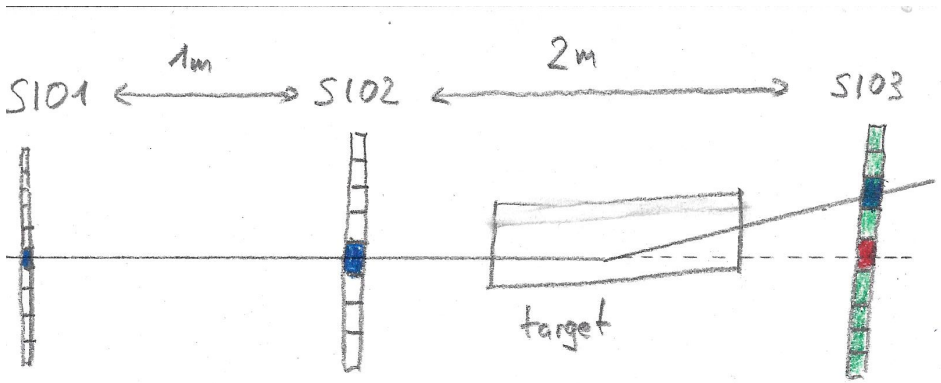
- TPC
  - Active target, 20 bar hydrogen, no gas amplification, 40 us drift time
  - Pad read out, up to 3 k channels – preamplifier + similar to MSADC system (12b x 2-5 MHz)
  - Muon looses about 100 kEv $\longrightarrow$ physics noise
  - Recoil Proton above 500 kEv
- Silicon
  - 3 stations before target $\longrightarrow$ strip or pixel detectors $\longrightarrow$ 12 k channels
  - 3-4 stations after target $\longrightarrow$ strip or pixel detectors $\longrightarrow$ 16k channels

Excpected PRM Data Rate:

- **Beam Intensity:** 5E7 muons/s
- **Event size (silicon only)**
  5E7 hits * 28 planes * 2 (cluster size) = 3E9 words/s = 12 GB/s
- **TPC:**
  detection of recoil protons
  expected rate 2kHz, threshold only (low information)
- **Trigger:**
  - Recoil proton rate: 2 kHz
    Bad Time resolution (40us gate)
  - Kink trigger or beam killer:
    reconstruction of tracks in silicon stations
    High efficiency and low purity $\rightarrow$ rate is dominated by background
    (maximum rate 1MHz) Good time resolution but 40us gate for TPC
- **Challenge:** matching muons track and TPC signal

kink trigger

use of Silicons or SciFis



- parallel readout of Silicons for trigger purpose
- silicon size 5x7 cm
- 1024/1280 stripes per plane
- silicon station has U,V,X,Y planes
- time resolution: sub nanosecond
- latency: not yet determined

Overview

Digital trigger:

- change of readout schema and TDCs for Trigger
- define requirements for trigger logic
- select development hardware for trigger logic
- rebuild current trigger logic on an timestamp approach
- developments and test in parallel to old trigger system

Proton radius measurement:

- low data rate threshold trigger from TPC $\approx 2\,\text{kHz}$
- additional geometrical trigger
  - kink trigger out of silicon detectors
  - beamkiller for veto tracks $<5\ \mu\text{rad}$

Challenge: matching TPC and kink trigger (40 us gate !)

$\rightarrow$ increase trigger latency up to 1 ms